# JNTUH COLLEGE OF ENGINEERING HYDERABAD
## M.Tech. (Embedded Systems) – Full Time w.e.f. 2015-16

## I – SEMESTER

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## III – SEMESTER

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## IV – SEMESTER

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</table>
Elective-I (ECE)
1. Digital System Design with PLDs
2. Advanced Data Communications
3. Advanced Digital Signal Processing

Elective-II (ECE)
1. VLSI Technology and Design
2. Coding Theory and Techniques
3. Speech and Audio Signal Processing

Elective-III (EEE)
1. Reliability Engineering
2. Intelligent Control
3. Sensors and Actuators

Elective-IV (CSE)
1. Embedded Real Time Operating Systems
2. Advanced Computer Architecture
3. Scripting Languages.

Elective-V (ECE)
1. Design of Fault Tolerant Systems
2. Embedded Networks
3. Image and Video processing

Elective-VI (ECE)
1. Hardware - Software Co-Design
2. Ad-hoc and Wireless Sensor Networks
3. Digital Signal Processors and Controllers

Elective-VII (EEE)
1. Modern Control Theory
2. Optimization Techniques
3. Robotics

Elective-VIII (CSE)
1. Network Security and Cryptography
2. Mobile Computing
3. High Speed Networks
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Embedded Systems)

EMBEDDED SYSTEMS DESIGN

Prerequisite: Microprocessor and Microcontrollers

Course Objectives:
1. To provide an overview of Design Principles of Embedded System.
2. To provide clear understanding about the role of firmware, operating systems in correlation with hardware systems.

Course Outcomes:
1. Expected to understand the selection procedure of Processors in the Embedded domain.
2. Design Procedure for Embedded Firmware.
3. Expected to visualize the role of Real time Operating Systems in Embedded Systems
4. Expected to evaluate the Correlation between task synchronization and latency issues

UNIT -I: Introduction to Embedded Systems

UNIT -II: Typical Embedded System:
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III: Embedded Firmware:
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV: RTOS Based Embedded System Design:
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V: Task Communication:
Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:
1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:
1. Embedded Systems - Raj Kamal, TMH.
4. An Embedded Software Primer - David E. Simon, Pearson Education.
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Embedded Systems)  
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DIGITAL CONTROL SYSTEMS

Prerequisite: Control Systems

Course Objectives:
- To explain basic and digital control system for the real time analysis and design of control systems.
- To apply the knowledge state variable analysis in the design of discrete systems.
- To explain the concept of stability analysis and design of discrete time systems.

Course Outcomes:
Upon the completion of this course, the student will be able to
- Apply the concepts of Digital control systems.
- Analyze and design of discrete systems in state variable analysis.
- To relate the concepts of stability analysis and design of discrete time systems.

UNIT – I: Concept & Representation of Discrete time Systems

Z-transform: Definition of Z-transforms – mapping between s-plane and z-plane – inverse z- transform – properties of z-transforms - ROC of z-transforms –pulse transfer function – relation between G(s) and G(z) – signal flow graph method applied to digital control systems.

UNIT- II: STATE SPACE ANALYSIS:

UNIT – III: Controllability, Observability & Stability tests
Concept of controllability, stabilizability, observability and reachability - Controllability and observability tests, Transformation of discrete time systems into controllable and observable forms.

UNIT- IV: Design of discrete time Controllers and observers
Design of discrete time controller with bilinear transformation – Realization of digital PID controller-Design of deadbeat controller; Pole placement through state feedback.

UNIT-V: STATE OBSERVERS:
Design of - Full order and reduced order observers. Study of observer based control design
TEXT BOOKS:

REFERENCES:
2. M. Gopal, Digital Control and State Variable Methods, TMH.
DIGITAL SYSTEM DESIGN WITH PLDs

(Elective – I)

Prerequisite: Switching Theory and Logic Design

Course Objectives:
1) To provide extended knowledge of digital logic circuits in the form of state model approach.
2) To provide an overview of system design approach using programmable logic devices.
3) To provide and understand of fault models and test methods.
4) To get exposed to the various architectural features of CPLDS and FPGAS.
5) To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6) To expose software tools used for design process with the help of case studies.

Course Outcomes:
1) To understands the minimization of Finite state machine.
2) To exposes the design approaches using ROM’s, PAL’s and PLA’s.
3) To provide in depth understanding of Fault models.
4) To understands test pattern generation techniques for fault detection.
5) To design fault diagnosis in sequential circuits.
6) To provide exposure to various CPLDS and FPGAS available in market.
7) To acquire knowledge in one hot state machine design applicable to FPGA.
8) To get exposure to EDA tools.
9) To provide understanding in the design of flow using case studies.

UNIT-I:
Programmable Logic Devices:
The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs- Altera CPLDs, FPGAs-FPGA technology, architecture, vortex CLB and slice- Stratix LAB and ALM-RAM Blocks, DSP Blocks, Clock Management, I/O standards, Additional features. [TEXTBOOK-1]

UNIT-II:
Analysis and derivation of clocked sequential circuits with state graphs and tables:
A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. [TEXTBOOK-2]

UNIT-III:
Sequential circuit Design:
Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]
UNIT-IV:
Fault Modeling and Test Pattern Generation:
Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model. Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT-V:
Fault Diagnosis in sequential circuits:
Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.1]

TEXTBOOKS:
1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
3. Logic Design Theory-N.N.Biswa,PHI

REFERENCES:
2. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Embedded Systems)  L   T    P    C  
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ADVANCED DATA COMMUNICATIONS  
(Elective – I)  

Prerequisite: Digital Communications  

Course Objectives:  
1. To learn about basics of Data Communication networks, different protocols, standards and layering concepts.  
2. To study about error detection and correction techniques.  
3. Know about link layer protocol and point to point protocols.  
4. To understand Medium Access Control sub layer protocols  
5. To know about Switching circuits, Multiplexing and Spectrum Spreading techniques for data transmission.  
6. To study Wired LANs different Ethernet standards  

Course Outcomes:  
At the end of the course, the student will be able to:  
1. Understand the concepts of Data Communication networks, different protocols, standards and layering.  
2. Acquire the knowledge of error detection, forward and reverse error correction techniques.  
3. Analyze link layer protocol and point to point protocols  
4. Explain and compare the performance of different MAC protocols like Aloha, CSMA, CSMA/CA, TDMA, FDMA & CDMA.  
5. Understand the features and the significance of Switching circuits, Multiplexing and Spectrum Spreading for data transmission.  
6. Understand the characteristics of Wired LANs and also the operation and applications of Connecting Devices  
7. Understand the services and functions of Network layer protocols.  

Unit I  
Data Communications, Networks and Network Types, Internet History, Standards and Administration, Protocol Layering, TCP/IP protocol suite, OSI Model. Digital Data Transmission, DTE-DCE interface.  

Data Link Layer  
Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol.  

Unit II  
Error Detection and Correction: Types of Errors, Redundancy, detection versus correction, Coding Block Coding: Error Detection, Vertical redundancy checks, longitudinal redundancy checks, Error Correction, Error correction single bit, Hamming code.  
Cyclic Codes: Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum  
Data Link Control: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol
Unit III
**Media Access Control (MAC) Sub Layer**
Random Access, Aloha, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation, Polling-Token Passing, Channelization - Frequency Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA).

Unit IV
**Switching:** Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of switch
**Multiplexing and Spectrum Spreading:** Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing, Spread Spectrum -Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum.

Unit V
**Wired LANS:** Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Giga bit Ethernet
**Connecting Devices:** Hubs, Link Layer Switches, Routers
**Networks Layer:** Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic Host Configuration Protocol (DHCP), Network Address Resolution(NATF), Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches.

**TEXT BOOKS:**
1. Data Communications and Networking - B. A. Forouzan, 5th, 2013, TMH.

**REFERENCE BOOKS:**
1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data Communications and Networking - B. A. Forouzan, 2nd, 2013, TMH.
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Embedded Systems) L T P C 4 0 0 4

ADVANCED DIGITAL SIGNAL PROCESSING
(Elective – I)

Prerequisite: Digital Signal Processing

Course Objectives:
The objectives of this course are to make the student
1. Understand the design of various types of digital filters and implement them using various implementation structures and study the advantages & disadvantages of a variety of design procedures and implementation structures.
2. understand the concept and need for Multirate signal Processing and their applications in various fields of Communication & Signal Processing
3. understand difference between estimation & Computation of Power spectrum and the need for Power Spectrum estimation.
4. Study various Parametric & Non parametric methods of Power spectrum estimation techniques and their advantages & disadvantages
5. Understand the effects of finite word/ register length used in hardware in implementation of various filters and transforms using finite precision processors.

Course Outcomes:
On completion of this course student will be able to
1. Design and implement a filter which is optimum for the given specifications.
2. Design a Mutirate system for the needed sampling rate and can implement the same using Polyphase filter structures of the needed order.
3. Estimate the power spectrum of signal corrupted by noise through a choice of estimation methods: Parametric or Non Parametric.
4. Can calculate the output Noise power of different filters due to various finite word length effects viz: ADC Quantization, product quantization, and can calculate the scaling factors needed to avoid Limit cycles: Zero input, overflow. Also they can decide the stability of the system by studying the effect due to coefficient quantization while implementing different filters and transforms.

UNIT –I:
Review of DFT, FFT, IIR Filters and FIR Filters.

UNIT -II:
Non-Parametric Methods:
Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman-Tukey methods, Comparison of all Non-Parametric methods

UNIT - III:
Parametric Methods:
UNIT –IV:
**Multi Rate Signal Processing**: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion. Examples of up-sampling using an All Pass Filter.

UNIT –V:
**Applications of Multi Rate Signal Processing**

TEXT BOOKS:
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.

REFERENCE BOOKS:
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Embedded Systems)                          L   T    P   C
VLSI TECHNOLOGY AND DESIGN                                     4    0    0   4
(Elective – II)

Prerequisite: VLSI, ICA

Course Objectives:
1) Students from other engineering background to get familiarize with large scale integration technology.
2) To expose fabrication methods, layout and design rules.
3) Learn methods to improve Digital VLSI system’s performance.
4) To know about VLSI Design constraints.
5) Visualize CMOS Digital Chip Design.

Course Outcomes:
1) Review of FET fundamentals for VLSI design.
2) To acquires knowledge about stick diagrams and layouts.
3) Enable to design the subsystems based on VLSI concepts.

UNIT –I: Review of Microelectronics and Introduction to MOS Technologies:

UNIT –II: Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III: Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV: Sequential Systems:
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V: Floor Planning:
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

REFERENCE BOOKS:
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Embedded Systems)  
CODING THEORY AND TECHNIQUES  
(Elective - II)

**Prerequisite:** Digital Communications

**Course Objectives:**
1. To acquire the knowledge in measurement of information and errors.
2. To study the generation of various code methods.
3. To study the various application of codes.

**Course Outcomes:**
1. Learning the measurement of information and errors.
2. Obtain knowledge in designing various codes like block codes, cyclic codes, convolution codes, turbo codes and space codes.

**UNIT – I:**
**Coding for Reliable Digital Transmission and storage**
Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

**Linear Block Codes:** Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system.

**UNIT – II:**
**Cyclic Codes** : Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

**UNIT – III:**
**Convolutional Codes** : Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority-logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

**UNIT – IV:**
**Turbo Codes**
LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

**UNIT – V:**
**Space-Time Codes**
Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti’s schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing : General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.
TEXT BOOKS:

REFERENCE BOOKS:
2. Digital Communications - Fundamental and Application - Bernard Sklar, PE.
4. Introduction to Error Control Codes - Salvatore Gravano - Oxford
SPEECH AND AUDIO SIGNAL PROCESSING
(Elective – II)

Prerequisite: Adaptive Signal Processing

Course Objectives:
The objectives of this course are to make the student
1. Understand the anatomy and Physiology of Speech Production system and perception
   model and to design an electrical equivalent of Acoustic model for Speech Production.
2. To understand the articulatory and acoustic interpretation of various phonemes and their
   allophones.
3. To analyze the speech in time domain and extract various time domain parameters
   which can be used for various applications like pitch extraction, end point detection,
   Speech Compression, Speech Synthesis etc.,
4. To study the concept of Homomorphic system and its use in extracting the vocal tract
   information from speech using Cepstrum which is a bye product of Homomorphic
   processing of Speech.
5. To study various Speech Signal Processing applications viz: Speech Enhancement,
   Speech Recognition, Speaker Recognition.
6. To study various Audio coding techniques based on perceptual modeling of the human
   ear.

Course Outcomes:
On completion of this course student will be able to
1. Model an electrical equivalent of Speech Production system.
2. Extract the LPC coefficients that can be used to Synthesize or compress the speech.
3. Design a Homomorphic Vocoder for coding and decoding of speech.
4. Enhance the speech and can design an Isolated word recognition system using HMM.
5. Can extract the features for Automatic speaker recognition system which can used for
   classification.
6. Can design basic audio coding methods for coding the audio signal.

Unit – I:
Fundamentals of Digital Speech Processing:
Anatomy & Physiology of Speech Organs, The Process of Speech Production, The Acoustic
theory of speech production- Uniform lossless tube model, effect of losses in vocal tract,
effect of radiation at lips, Digital models for speech signals.

Perception: Anatomical pathways from the Ear to the Perception of Sound, The Peripheral
Block schematics of the Peripheral Auditory system.

Unit – II:
Time Domain models for Speech Processing:
Introduction – Window considerations, Short time energy, average magnitude, average zero
crossing rate, Speech vs Silence discrimination using energy and zero crossing, pitch period
estimation using a parallel processing approach, the short time autocorrelation function,
average magnitude difference function, pitch period estimation using the autocorrelation
function.
Linear Predictive Coding (LPC) Analysis:

Unit – III:
Homomorphic Speech Processing:

Speech Enhancement:

Unit – IV:
Automatic Speech Recognition:
Basic pattern recognition approaches, parametric representation of Speech, Evaluating the similarity of Speech patterns, Isolated digit Recognition System, Continuous word Recognition system. Elements of HMM, Training & Testing of Speech using HMM.

Automatic Speaker Recognition:
Recognition techniques, Features that distinguish speakers, MFCC, delta MFCC, Speaker Recognition Systems: Speaker Verification System, Speaker Identification System, Performance Metrics.

Unit – V:
Audio Coding:

TEXT BOOKS:

REFERENCE BOOKS:
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Embedded Systems)  

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RELIABILITY ENGINEERING  
(Elective- III)

Prerequisite: None

Course Objectives:
1. To comprehend the concept of Reliability and Unreliability
2. Derive the expressions for probability of failure, Expected value and standard deviation of Binominal distribution, Poisson distribution, normal distribution and weibull distributions.
3. Formulating expressions for Reliability analysis of series-parallel and Non-series parallel systems

Course Outcomes: Upon the completion of this course, the student will be able to
1. Apply fundamental knowledge of Reliability to modeling and analysis of series-parallel and Non-series parallel systems.
3. Understand or become aware of various failures, causes of failures and remedies for failures in practical systems.

Unit I:

Unit II:

Unit III:
Classification of engineering systems: series, parallel and series-parallel systems-
Expressions for the reliability of the basic configurations.
Reliability evaluation of Non-series-parallel configurations: Decomposition, Path based and cutest based methods, Deduction of the Paths and cut sets from Event tree.

Unit IV:
Discrete Markov Chains: General modeling concepts, stochastic transitional probability matrix, time dependent probability evaluation and limiting state probability evaluation of one component repairable model. Absorbing states.
UNIT-V:
Approximate system Reliability analysis of Series systems, parallel systems with two and more than two components, Network reduction techniques. Minimal cutset/failure mode approach.

TEXT BOOKS:

REFERENCES:
INTELLIGENT CONTROL
(Elective-III)

Prerequisite: None

Course Objectives:
1. Gaining an understanding of the functional operation of a variety of intelligent control techniques and their bio-foundations
2. The study of control-theoretic foundations
3. Learning analytical approaches to study properties

Course Outcomes:
Upon the completion of this course, the student will be able to
1. Develop Neural Networks, Fuzzy Logic and Genetic algorithms.
2. Implement soft computing to solve real-world problems mainly pertaining to control system applications

Unit-I

Unit-II
Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feedforward Multilayer Perceptron. Learning and Training the neural network. Data Processing: Scaling, Fourier transformation, principal-component analysis.

Unit-III

Unit-IV
Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters. Solution of typical control problems using genetic algorithm. Concept on some other search techniques like tabu search and ant-colony search techniques for solving optimization problems.

Unit-V
Text Books:

References:
SENSORS AND ACTUATORS
(Elective – III)

Prerequisite: None

Course Objectives:
1. To Learn about Electro mechanical sensors.
2. To Learn the use of the thermal sensors and magnetic sensors for embedded system.
3. To learn the basics of radiation sensors, smart sensors and actuators.

Course Outcomes:
1. Students will gain knowledge to interface various sensors and actuators in embedded applications.

UNIT - I: Sensors / Transducers
Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization.

Mechanical and Electromechanical Sensors

UNIT – II: Thermal Sensors

Magnetic sensors

UNIT - III: Radiation Sensors
Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors.

Electro analytical Sensors
UNIT - IV: Smart Sensors

Sensors –Applications

UNIT - V: Actuators

TEXT BOOKS:
EMBEDDED REAL TIME OPERATING SYSTEMS
(Descriptive – IV)

Prerequisite: Computer Organization and Operating System

Course Objectives:
1. To provide broad understanding of the requirements of Real Time Operating Systems.
2. To make the student understand, applications of these Real Time features using case studies.

Course Outcomes:
1. Be able to explain real-time concepts such as preemptive multitasking, task priorities, priority inversions, mutual exclusion, context switching, and synchronization, interrupt latency and response time, and semaphores.
2. Able describe how a real-time operating system kernel is implemented.
3. Able explain how tasks are managed.
4. Explain how the real-time operating system implements time management.
5. Discuss how tasks can communicate using semaphores, mailboxes, and queues.
6. Be able to implement a real-time system on an embedded processor.
7. Be able to work with real time operating systems like RT Linux, Vx Works, MicroC /OS-II, Tiny Os

UNIT – I: Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II: Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III: Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV: Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V: Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOKS:

REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Embedded Systems)  
ADVANCED COMPUTER ARCHITECTURE  
(Effective – IV)

Prerequisite: Computer Organization and Operating System

Course Objectives:
1. Explains instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
2. Explains different classifications of instruction set architectures
3. Explains the advanced concepts such as instruction level parallelism, out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction
4. Examine software support for ILP, including VLIW and similar approaches
5. Teach memory hierarchy design issues, including caching and virtual memory approaches
6. Explains multiprocessor and parallel processing architectures
7. Gives the organization and design of contemporary processor architectures
8. As the current trend in computer architecture is towards chip-multiprocessing, the architecture of shared memory multiprocessors and chip level interconnect (network-on-chip) will be covered as future scope.

Course Outcomes:
A student who has met the objectives of the course will be able to:
1. Understand advanced computer architecture aspects
2. Describe and explain instruction level parallelism with static scheduling, out-of-order execution and network-on-chip architectures
3. Understand the architecture and limitations of chip-multiprocessing
4. Explain in detail about time-predictable computer architecture
5. Understand the operation of modern CPUs including pipelining, memory systems and busses.
6. Design and emulate a single cycle or pipelined CPU by given specifications using Hardware Description Language (HDL).
7. Write reports and make presentations of computer architecture projects

UNIT- I: Fundamentals of Computer Design
Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II: Pipelines
Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design
UNIT - III: Instruction Level Parallelism the Hardware Approach
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo’s approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach
Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT – IV:
Multi Processors and Thread Level Parallelism
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V:
Inter Connection and Networks
Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture
Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

REFERENCE BOOKS:
SCRIPTING LANGUAGES
( Elective – IV)

Prerequisite: C Language Programs

Course Objectives:
The goal of the course is to study:
1. The principles of scripting languages.
2. Motivation for and applications of scripting.
3. Difference between scripting languages and non-scripting languages.
4. Types of scripting languages.
5. Scripting languages such as PERL, TCL/TK, python and BASH.
6. Creation of programs in the Linux environment.
7. Usage of scripting languages in IC design flow.

Course Outcomes:
Upon learning the course, the student will have the:
1. Ability to create and run scripts using PERL/TCl/Python in IC design flow.
2. Ability to use Linux environment and write programs for automation of scripts in VLSI tool
design flow.

Unit – 1 : Linux Basics
Introduction to Linux, File System of the Linux, General usage of Linux kernel & basic
commands, Linux users and group, Permissions for file, directory and users, searching a file
& directory, zipping and unzipping concepts.

Unit – 2 : Linux Networking
Introduction to Networking in Linux, Network basics & Tools, File Transfer Protocol in Linux,
Network file system, Domain Naming Services, Dynamic hosting configuration Protocol &
Network information Services.

Unit – 3 : Perl Scripting
Introduction to Perl Scripting, working with simple values, Lists and Hashes, Loops and
Decisions, Regular Expressions, Files and Data in Perl Scripting, References & Subroutines,
Running and Debugging Perl, Modules, Object – Oriented Perl.

Unit – 4 : Tcl / Tk Scripting
Tcl Fundamentals, String and Pattern Matching, Tcl Data Structures, Control Flow
Commands, Procedures and Scope, Evel, Working with Unix, Reflection and Debugging,
Script Libraries, Tk Fundamentals, Tk by examples, The Pack Geometry Manager, Binding
Commands to X Events, Buttons and Menus, Simple Tk Widgets, Entry and List box Widgets
Focus, Grabs and Dialogs.

Unit – 5 : Python Scripting
Introduction to Python, using the Python Interpreter, More Control Flow Tools, Data
Structures, Modules, Input and Output, Errors and Exceptions, Classes, Brief Tour of the
Standard Library.
Text Books:
1. Python Tutorial by Guido Van Rossum, Fred L. Drake Jr. editor, Release 2.6.4
2. Practical Programming in Tcl and Tk by Brent Welch, Updated for Tcl 7.4 and Tk 4.0.
3. Teach Yourself Perl in 21 days by David Till.

Reference Books:
List of Experiments:

1. **Functional Testing Of Devices**
   Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.

2. **Exporting Display On To Other Systems**
   Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.

3. **GPIO Programming**
   Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.

4. **Interfacing Chronos eZ430**
   Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.

5. **ON/OFF Control Based On Light Intensity**
   Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.

6. **Battery Voltage Range Indicator**
   Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)

7. **Dice Game Simulation**
   Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.

8. **Displaying RSS News Feed On Display Interface**
   Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.

9. **Porting Openwrt To the Device**
   Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.

10. **Hosting a website on Board**
    Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server(eg: Apache) and thereby host the website.

11. **Webcam Server**
    Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.

12. **FM Transmission**
    Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

**Note:** Devices mentioned in the above lists include Arduino, Raspberry Pi, Beaglebone
SYSTEM ON CHIP ARCHITECTURE

Prerequisite: Embedded System Design.

Course Objectives:
1) To introduce the architectural features of system on chip.
2) To provides information on interconnection necessities between computational block and memory block.

Course Outcomes:
1) Introduction to SOC Architecture and design.
2) Processor design Architectures and limitations
3) To acquires the knowledge of memory architectures on SOC.
4) To understands the interconnection strategies and their customization on SOC.

UNIT – I: Introduction to the System Approach

UNIT – II: Processors

UNIT – III: Memory Design for SOC:

UNIT - IV: Interconnect Customization and Configuration

UNIT – V: Application Studies / Case Studies
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JEPG compression.

TEXT BOOKS:
REFERENCE BOOKS:
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM
EMBEDDED PROGRAMMING

Prerequisite: C Language Programs

Course Objectives:
1. To explore the difference between general purpose programming languages and Embedded Programming Language.
2. To provide case studies for programming in Embedded systems.

Course Outcomes:
1. Expected to learn the basics of Embedded C with reference to 8051.
2. Understand how to handle control and data pins at hardware level.
3. Capable of introducing into objective nature of Embedded C.
4. Understand the specifications of real time embedded programming with case studies.

UNIT – I: Programming Embedded Systems in C
Introduction, What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

UNIT – II: Reading Switches
Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT – III: Adding Structure to your Code
Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV: Meeting Real-Time Constraints
Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V: Case Study: Intruder Alarm System
Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:
1. Embedded C by Michael J. Pont, A Pearson Education

REFERENCE BOOKS:
1. PICmicro MCU C-An introduction to programming, The Microchip PIC in CCS C By Nigel Gardner
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M.Tech. I Year II-Sem (Embedded Systems)                              L   T    P   C
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DESIGN OF FAULT TOLERANT SYSTEMS
(Elective – V)

Prerequisite: Digital System Design with PLDS

Course Objectives:
1) To provide or broad understanding of fault diagnosis and tolerant design Approach.
2) To illustrate the framework of test pattern generation using semi and full automatic
   approach.

Course Outcomes:
1) To acquire the knowledge of fundamental concepts in fault tolerant design.
2) Design requirements of self check-in circuits
3) Test pattern generation using LFSR
4) Design for testability rules and techniques for combinational circuits
5) Introducing scan architectures.

UNIT-I: Fault Tolerant Design:
Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.
Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts. [TEXTBOOK-1]

UNIT-II: Self Checking circuits & Fail safe Design:
Self Checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.
Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design. [TEXTBOOK-1]

UNIT-III: Design for Testability:
Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller’s expansion technique, use of control and syndrome testable designs.
Design for testability by means of scan:
Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.[TEXTBOOK-2]

UNIT-IV: Logic Built-in-self-test:
BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA’s, One’s counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralized and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self –testing using MISR and SRS6, Concurrent BIST, BILBO, Enhancing
coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results. [TEXTBOOK-2]

UNIT-V: Standard IEEE Test Access Methods:
Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language. [TEXTBOOK-2]

TEXTBOOKS:
1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala, 1984, PHI

REFERENCES:
1. Digital Systems Testing and Testable Design-Miron Abramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books
EMBEDDED NETWORKS  
(Selective – V)

Prerequisite: Computer Networks.

Course Objectives:
1. To elaborate on the conceptual frame work of physical layer and topological issues of networking in Embedded Systems.
2. To emphasis on issues related to guided and unguided media with specific reference to Embedded device level connectivity.

Course Outcomes:
1. Expected to acquire knowledge on communication protocols of connecting Embedded Systems.
2. Expected to master the design level parameters of USB and CAN bus protocols.
3. Understand the design issues of Ethernet in Embedded networks.
4. Acquire the knowledge of wireless protocols in Embedded domain.

UNIT –I: Embedded Communication Protocols:  

UNIT –II: USB and CAN Bus:  

UNIT –III: Ethernet Basics:  

UNIT –IV: Embedded Ethernet:  

UNIT –V: Wireless Embedded Networking:  
TEXT BOOKS:

REFERENCE BOOKS:
1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
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M.Tech. I Year II-Sem (Embedded Systems)  L  T  P  C
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IMAGE AND VIDEO PROCESSING
(Elective - V)

Prerequisite: Digital Image Processing

Course Objectives:
1. The student will be able to understand the quality improvement methods of Image.
2. To study the basic digital image and video filter operations.
3. Understand the fundamentals of Image Compression.
4. Understand the representation of video.
5. Understand the principles and methods of motion estimation.

Course Outcomes:
1. The students will learn image representation, filtering, compression.
2. Students will learn the basics of video processing, representation, motion estimation.

UNIT – I: Fundamentals of Image Processing and Image Transforms
Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.

Image Segmentation
Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT – II: Image Enhancement

UNIT – III: Image Compression
Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Bit plane coding, Transform coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT - IV: Basic Steps of Video Processing

UNIT – V: 2-D Motion Estimation
Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.
TEXT BOOKS:

REFERENCE BOOKS:
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year II-Sem (Embedded Systems)  

HARDWARE - SOFTWARE CO-DESIGN  
(Elective – VI)

Prerequisite: Advanced Computer Architecture, Embedded System Design.

Course Objective:  
1) To provide a broad understanding of the specific requirement of Hardware and software integration for embedded system

Course Outcomes:  
1) To acquire the knowledge on various models  
2) To explore the interrelationship between Hardware and software in a embedded system  
3) Acquire the knowledge of firmware development process and tools  
4) Understand validation methods and adaptability.

UNIT –I:  
Co-Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.  
Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT –II:  
Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures:  
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:  
Compilation Techniques and Tools for Embedded Processor Architectures:  
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:  
Design Specification and Verification:  
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:  
Languages for System – Level Specification and Design-I:  
System – level specification, design representation for system level synthesis, system level specification languages,  
Languages for System – Level Specification and Design-II:  
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.
TEXT BOOKS:

REFERENCE BOOKS:
1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer
AD-HOC AND WIRELESS SENSOR NETWORKS
(Elective - VI)

Prerequisite: Wireless Sensor Networks.

Course Objectives:
1. To study the fundamentals of wireless Ad-Hoc Networks.
2. To study the operation and performance of various Ad-hoc wireless network protocols.
3. To study the architecture and protocols of Wireless sensor networks.

Course Outcomes:
1. Students will be able to understand the basis of Ad-hoc wireless networks.
2. Students will be able to understand design, operation and the performance of MAC layer protocols of Adhoc wireless network.
3. Students will be able to understand design, operation and the performance of routing protocol of Adhoc wireless network.
4. Students will be able to understand design, operation and the performance of transport layer protocol of Adhoc wireless networks.
5. Students will be able to understand sensor network Architecture and will be able to distinguish between protocols used in Adhoc wireless network and wireless sensor networks.

UNIT - I:
Wireless LANs and PANs

AD HOC WIRELESS NETWORKS
Introduction, Issues in Ad Hoc Wireless Networks.

UNIT - II:
MAC Protocols

UNIT - III:
Routing Protocols

UNIT – IV:
Transport Layer Protocols
Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of
Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT – V:
Wireless Sensor Networks

TEXT BOOKS:

REFERENCE BOOKS:
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M.Tech. I Year II-Sem (Embedded Systems)  

DIGITAL SIGNAL PROCESSORS AND CONTROLLERS  
(Elective – VI)

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Prerequisite: Microprocessors and Micro Controllers

Course Objectives:
1. To provide a comprehensive understanding of various programs of DSP Processors.
2. To distinguish between the architectural difference of ARM and DSPs along with floating point capabilities.

Course Outcomes:
The students are
1. Expected to learn various DSPs and their architectural features.
2. Explore the ARM development towards the functional capabilities of DS Processing.
3. Expected to work with ASM level program using the instruction set.
4. To explore the selection criteria of DSP / ARM processors by understanding the functional level trade off issues.

UNIT-I: Introduction to Digital Signal Processing:
Introduction, A digital Signal – Processing system, the sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation.

Architectures for Programmable DSP devices:
Basic Architectural features, DSP computational building blocks, Bus Architecture and Memory, Data addressing capabilities, Address generation UNIT, programmability and program execution, speed issues, features for external interfacing. [TEXTBOOK-1]

UNIT-II: Programmable Digital Signal Processors:
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX processors, memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, On-Chip peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX processors. [TEXTBOOK-1]

UNIT-III: Architecture of ARM Processors:
Introduction to the architecture, Programmer’s model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

Technical Details of ARM Processors:
General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility. [TEXTBOOK-2]
UNIT-IV: Instruction SET: Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming. [TEXTBOOK-2]

UNIT-V: Floating Point Operations: About Floating Point Data, Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1.

ARM Cortex-M4 and DSP Applications:
DSP on a microcontroller, Dot Product example, writing optimised DSP code for the Cortex-M4-Biquad filter, Fast Fourier transform, FIR filter. [TEXTBOOK-2]

TEXTBOOKS:

REFERENCES:
MODERN CONTROL THEORY
(Elective – VI)

Prerequisite: Control Systems

Course Objectives:
1. To explain the concepts of basics and modern control system for the real time analysis and design of control systems.
2. To explain the concepts of state variables analysis.
3. To study and analyze non linear systems.
4. To analyze the concept of stability for nonlinear systems and their categorization.
5. To apply the comprehensive knowledge of optimal theory for Control Systems.

Course Outcomes:
Upon completion of this course, students should be able to:
1. Various terms of basic and modern control system for the real time analysis and design of control systems.
2. To perform state variables analysis for any real time system.
3. Apply the concept of optimal control to any system.
4. Able to examine a system for its stability, controllability and observability.
5. Implement basic principles and techniques in designing linear control systems.
6. Formulate and solve deterministic optimal control problems in terms of performance indices.
7. Apply knowledge of control theory for practical implementations in engineering and network analysis.

UNIT I: Mathematical Preliminaries and State Variable Analysis:

UNIT II: Controllability and Observability:
General concept of controllability – Controllability tests, different state transformations such as diagonalization, Jordon canonical forms and Controllability canonical forms for Continuous-Time Invariant Systems – General concept of Observability – Observability tests for Continuous-Time Invariant Systems – Observability of different State transformation forms.

UNIT III: State Feedback Controllers and Observers:
State feedback controller design through Pole Assignment, using Ackkermans formula–State observers: Full order and Reduced order observers.
UNIT IV: Non-Linear Systems:

UNIT V: Stability Analysis:

TEXT BOOKS:
1. M.Gopal, Modern Control System Theory, New Age International - 1984

REFERENCES:
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M.Tech. I Year II-Sem (Embedded Systems) (Elective- VII )

OPTIMIZATION TECHNIQUES

Prerequisite: None

Course Objectives:
1. To understand the theory of optimization methods and algorithms developed for solving various types of optimization problems.
2. To develop an interest in applying optimization techniques in problems of Engineering and Technology
3. To apply the mathematical results and numerical techniques of optimization theory to concrete Engineering problems.

Course Outcomes:
Upon the completion of this course, the student will be able to
1. Know basic theoretical principles in optimization
2. formulate optimization models and obtain solutions for optimization;
3. apply methods of sensitivity analysis and analyze post processing of results

UNIT – I
Introduction and Classical Optimization Techniques:

Classical Optimization Techniques

UNIT – II
Linear Programming

UNIT – III
Transportation Problem
Finding initial basic feasible solution by north – west corner rule, least cost method and Vogel’s approximation method – testing for optimality of balanced transportation problems.

Unconstrained Nonlinear Programming:
One – dimensional minimization methods: Classification, Fibonacci method and Quadratic interpolation method

UNIT – IV
Unconstrained Optimization Techniques
Uni-variate method, Powell’s method and steepest descent method.
Constrained Nonlinear Programming:
Characteristics of a constrained problem, Classification, Basic approach of Penalty Function method; Basic approach of Penalty Function method; Basic approaches of Interior and Exterior penalty function methods. Introduction to convex Programming Problem.

UNIT – V
Dynamic Programming:

TEXT BOOKS:

REFERENCES:
4. Linear Programming by G. Hadley
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ROBOTICS
(Elective – VII)

Prerequisite:
Introduction to Signals, Systems & Circuits
Analytical Foundations of Electronics and Communication Engineering,
Linear Systems
Elements of Control

Course Objectives:
1. This introductory course is valuable for students who wish to learn about robotics through a study of industrial robot systems analysis and design.
2. This course is suited to students from engineering and science backgrounds that wish to broaden their knowledge through working on a subject that integrates multi-disciplinary technologies.

Course Outcomes:
Upon the completion of this course, the student will be able to:
1. Describe the various elements that make an industrial robot system
2. Discuss various applications of industrial robot systems
3. Analyze robot manipulators in terms of their kinematics, kinetics, and control
4. Model robot manipulators and analyze their performance, through running simulations using a MATLAB-based Robot Toolbox
5. Select an appropriate robotic system for a given application and discuss the limitations of such a system
6. Program and control an industrial robot system that performs a specific task.

UNIT - I: Introduction & Basic Definitions
History pf robots-robot anatomy, Coordinate Systems , Human arm Characteristics ,
Cartesian , Cylindrical, Polar, coordinate frames , mapping transform.

UNIT - II: Kinematics – Inverse Kinematics
Kinematics , Mechanical structure and notations , description of links and joints , Denavit
Hatenberg notation , manipulator transformation matrix , examples inverse kinematics.

Velocity Propagation along links, manipulator Jacobian – Jacobian singularities – Lagrange
Euler formulation Newton Euler formulation basics of trajectory planning.

Hydraulic and Electrical Systems Including Pumps, valves, solenoids, cylinders, stepper
motors, Encoders and AC Motors Range and use of sensors, Microswitches, Resistance
Transducers, Piezo-electric, Infrared and Lasers Applications of Sensors : Reed Switches,
Ultrasonic, Barcode Readers and RFID – Fundamentals of Robotic vision.

UNIT - V: Robots and Applications.
Industrial Applications – Processing applications – Assembly applications, Inspection
applications , Non Industrial applications.
TEXT BOOKS:
3. Introduction to Robotics – S. Nikv, 2001, Prentice Hall,

REFERENCE BOOKS:
Prerequisite: None

Course Objectives:
1. Understand the basic concept of Cryptography and Network Security, their mathematical models
2. To provide deeper understanding of application to network security, threats/vulnerabilities to networks and countermeasures
3. To create an understanding of Authentication functions the manner in which Message Authentication Codes and Hash Functions works
4. To provide familiarity in Intrusion detection and Firewall Design Principles

Course Outcomes:
After completion of this course, the student shall be able to:
1. Describe computer and network security fundamental concepts and principles
2. Identify and assess different types of threats, malware, spyware, viruses, vulnerabilities
3. Encrypt and decrypt messages using block ciphers
4. Describe the inner-workings of today's remote exploitation and penetration techniques
5. Describe the inner-workings of popular encryption algorithms, digital signatures, certificates, anti-cracking techniques, and copy-right protections
6. Demonstrate the ability to select among available network security technology and protocols such as IDS, IPS, firewalls, SSL, SSH, IPSec, TLS, VPNs, etc.
7. Analyze key agreement algorithms to identify their weaknesses


UNIT - IV: Message Authentication and Hash Functions
Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm.
Authentication Applications: Kerberos, Electronic Mail Security: Pretty Good Privacy, S/MIME.


Intruders, Viruses and Worms: Intruders, Viruses and Related threats.

Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

REFERENCE BOOKS:
1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
5. Introduction to Cryptography, Buchmann, Springer.
MOBILE COMPUTING
(Elective – VIII)

Prerequisites:
1. Computer Networks
2. Distributed Systems OR Distributed Operating Systems OR Advanced Operating Systems

Course Objectives:
1. To make the student understand the concept of mobile computing paradigm, its novel applications and limitations.
2. To understand the typical mobile networking infrastructure through a popular GSM protocol
3. To understand the issues and solutions of various layers of mobile networks, namely MAC layer, Network Layer & Transport Layer
4. To understand the database issues in mobile environments & data delivery models.
5. To understand the ad hoc networks and related concepts.
6. To understand the platforms and protocols used in mobile environment.

Course Outcomes:
1. Able to think and develop new mobile application.
2. Able to take any new technical issue related to this new paradigm and come up with a solution(s).
3. Able to develop new ad hoc network applications and/or algorithms/protocols.
4. Able to understand & develop any existing or new protocol related to mobile environment

UNIT – I

UNIT – II
(Wireless) Medium Access Control (MAC) : Motivation for a specialized MAC (Hidden and exposed terminals, Near and far terminals), SDMA, FDMA, TDMA, CDMA, Wireless LAN/(IEEE 802.11)
Mobile Network Layer : IP and Mobile IP Network Layers, Packet Delivery and Handover Management, Location Management, Registration, Tunneling and Encapsulation, Route Optimization, DHCP.

UNIT – III
UNIT IV
Data Dissemination and Synchronization: Communications Asymmetry, Classification of Data Delivery Mechanisms, Data Dissemination, Broadcast Models, Selective Tuning and Indexing Methods, Data Synchronization – Introduction, Software, and Protocols

UNIT V
Mobile Ad hoc Networks (MANETs): Introduction, Applications & Challenges of a MANET, Routing, Classification of Routing Algorithms, Algorithms such as DSR, AODV, DSDV, Mobile Agents, Service Discovery.

Text Books:

REFERENCE BOOKS:
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HIGH SPEED NETWORKS (Elective-VIII)

Prerequisite: Computer Networks

Course Objectives:
At the end of the course, the students will be able to:
1. understand of switching and data transmission.
2. Familiarize the students with the error correction and detection techniques.
3. Understanding of basic principles of Multiple Access, Frame Relay and ATM
4. Obtain the knowledge of Logical Addressing, Transport layer protocols, congestion control mechanism and Domain Name System
5. Gain an expertise in areas like Logical Network Design and routing protocols.

Course Outcomes:
After completing this course the student must demonstrate the knowledge and ability to
1. Independently understand the basic data transmission and data link layer concepts.
2. Understand and explain error correction and detection.
3. Analyze the details of network layer protocols and transport layer protocols
4. Design different types of network topologies.
5. Analyze and compare various routing protocols.

UNIT I
Switching and Data Transmission
ISO-OSI reference model. TCP/IP reference model, Circuit-switched networks, Datagram networks, Virtual-circuit networks, Structure of a switch, Telephone network, Dial-up modems, Digital Subscriber line, Cable TV networks

Data Link Layer
Error Detection and Correction: Introduction, Block coding, Linear Block codes, Cyclic codes, Checksum -  Data Link Control: Framing, Flow and Error control, Protocols, Noiseless channels, Noisy channels, HDLC, Point-to-Point Protocol

UNIT II
Multiple Access: Random Access, Controlled Access, Channelization – Connecting Devices: Connecting LANs, Backbone Networks, Virtual LANs.

High Speed Networks
Frame Relay: Packet-Switching Networks, Frame Relay Networks – Asynchronous Transfer Mode (ATM) : ATM Protocol Architecture, ATM Logical Connections, ATM Cells, ATM Service Categories, ATM Adaptation Layer (AAL) - High-Speed LANs : The Emergence of High-Speed LANs, Ethernet, Fiber Channel, Wireless LANs.

UNIT III
Network Layer

Transport Layer and Application Layer
UNIT IV
Domain Name System: Name space, Domain Name Space, Distribution of Name Space, DNS in the internet, Resolution, DNS messages, E-mail

Needs and Goals for Network Design
Analyzing Business Goals and Constraints: Using a Top-Down Network Design
Constraints, Analyzing Business Goals, Analyzing Business constraints – Analyzing
Characterizing Network Traffic: Characterizing Traffic Flow, Traffic Load, Traffic Behavior, Quality of Service Requirements

UNIT V
Logical Network Design
Designing Network Design: Hierarchical Network Design, Redundant Network Design
Topologies, Modular Network Design, Designing a Campus Network Design Topology, Designing the Enterprise Edge Topology, Secure Network Design Topologies

Designing Models for Addressing and Naming: Guidelines for Assigning Network Layer
Addresses, Using a Hierarchical Model for Assigning Addresses, Designing a Model for
Naming.

Selecting Switching and Routing Protocols
Selecting Bridging & Switching Protocols, Spanning Tree Protocol Enhancements -
Selecting Routing Protocols: Characterizing Routing protocols, IP Routing, Novell
NetWare Routing, Using Multiple Routing Protocols in an Internet work

Text Books:
1. Data Communications and Networking, Behrouz A. Forouzan, Fourth Edition, Tata
McGraw Hill
2. High Speed Networks and Internets – Performance and Quality of Service, William
(CISCO Press)

Reference Books:
Thomson.
4. Campus Network Design Fundamentals, Diane Teare, Catherine Paquet, Pearson
Education (CISCO Press)
5. Computer Communications Networks, Mir, Pearson Education.
List of Programs:

1. Write a simple program to print “hello world”
2. Write a simple program to show a delay.
3. Write a loop application to copy values from P1 to P2
4. Write a c program for counting the no of times that a switch is pressed & released.
5. Illustrate the use of port header file (port M) using an interface consisting of a keypad and liquid crystal display.
6. Write a program to create a portable hardware delay.
7. Write a c program to test loop time outs.
8. Write a c program to test hardware based timeout loops.
9. Develop a simple EOS showing traffic light sequencing.
10. Write a program to display elapsed time over RS-232 link.
11. Write a program to drive SEOS using Timer 0.
12. Develop software for milk pasteurization system.

Mini Project

Develop & implement a program for intruder alarm system.
SOFT SKILLS LAB
(Activity-based)

Course Objectives
- To improve the fluency of students in English
- To facilitate learning through interaction
- To illustrate the role of skills in real-life situations with case studies, role plays etc.
- To train students in group dynamics, body language and various other activities which boost their confidence levels and help in their overall personality development
- To encourage students develop behavioral skills and personal management skills
- To impart training for empowerment, thereby preparing students to become successful professionals

Learning Outcomes
- Developed critical acumen and creative ability besides making them industry-ready.
- Appropriate use of English language while clearly articulating ideas.
- Developing insights into Language and enrich the professional competence of the students.
- Enable students to meet challenges in job and career advancement.

INTRODUCTION
Definition and Introduction to Soft Skills – Hard Skills vs Soft Skills – Significance of Soft/Life/Self Skills – Self and SWOT Analysis

1. Exercises on Productivity Development
   - Effective/Assertive Communication Skills (Activity based)
   - Time Management (Case Study)
   - Creativity & Critical Thinking (Case Study)
   - Decision Making and Problem Solving (Case Study)
   - Stress Management (Case Study)

2. Exercises on Personality Development Skills
   - Self-esteem (Case Study)
   - Positive Thinking (Case Study)
   - Emotional Intelligence (Case Study)
   - Team building and Leadership Skills (Case Study)
   - Conflict Management (Case Study)

3. Exercises on Presentation Skills
   - Netiquette
   - Importance of Oral Presentation – Defining Purpose- Analyzing the audience-
     Planning Outline and Preparing the Presentation- Individual & Group
     Presentation- Graphical Organizers- Tools and Multi-media Visuals
   - One Minute Presentations (Warming up)
   - PPT on Project Work- Understanding the Nuances of Delivery- Body
     Language – Closing and Handling Questions – Rubrics for Individual
     Evaluation (Practice Sessions)

4. Exercises on Professional Etiquette and Communication
   - Role-Play and Simulation- Introducing oneself and others, Greetings,
     Apologies, Requests, Agreement & Disagreement….etc.
5. **Exercises on Ethics and Values**

- Introduction — Types of Values - Personal, Social and Cultural Values - Importance of Values in Various Contexts
- Significance of Modern and Professional Etiquette – Etiquette (Formal and Informal Situations with Examples)
- Attitude, Good Manners and Work Culture (Live Examples)
- Social Skills - Dealing with the Challenged (Live Examples)
- Professional Responsibility – Adaptability (Live Examples)
- Corporate Expectations

*Note: Hand-outs are to be prepared and given to students.*

*Training plan will be integrated in the syllabus.*

*Topics mentioned in the syllabus are activity-based.*

**SUGGESTED SOFTWARE:**

- The following software from ‘train2success.com’
  - Preparing for being Interviewed
  - Positive Thinking
  - Interviewing Skills
  - Telephone Skills
  - Time Management
  - Team Building
  - Decision making

**SUGGESTED READING:**

12. *The Hindu Speaks on Education* by the Hindu Newspaper