JNTUH COLLEGE OF ENGINEERING HYDERABAD
(AUTONOMOUS)
M.Tech. (Digital Systems & Computer Electronics) – Full Time w.e.f. 2018-19

SEMESTER - I

S. No.	Course Type	Course Title	L	T	P	Credits
1	Core 1	Digital Systems Design with PLDs	3	0	0	3
2	Core 2	VLSI Technology and Design	3	0	0	3
3	P E - 1	Professional Elective - 1	3	0	0	3
4	P E - 2	Professional Elective - 2	3	0	0	3
5	Lab 1	Digital Systems Design Lab	0	0	4	2
6	Lab 2	Scripting Languages Lab	0	0	4	2
7		Research Methodology and IPR	2	0	0	2
8	Aud 1	Audit Course 1	2	0	0	0
		Total Credits	**16**	**0**	**8**	**18**

SEMESTER - II

S. No.	Course Type	Course Title	L	T	P	Credits
1	Core 3	Advanced Computer Architectures	3	0	0	3
2	Core 4	Design of Fault Tolerant Systems	3	0	0	3
3	P E – 3	Professional Elective – 3	3	0	0	3
4	P E – 4	Professional Elective – 4	3	0	0	3
5	Lab 3	Embedded Systems Lab	0	0	4	2
6	Lab 4	Simulation Lab	0	0	4	2
7		Mini Project with Seminar	0	0	4	2
8	Aud 2	Audit Course 2	2	0	0	0
		Total Credits	**16**	**0**	**8**	**18**

SEMESTER - III

S. No.	Course Type	Course Title	L	T	P	Credits
1	P E – 5	Professional Elective – 5	3	0	0	3
2	O E	Open Elective	3	0	0	3
3	Dissertation	Dissertation Phase - I	0	0	20	10
		Total	**06**	**0**	**20**	**16**

SEMESTER - IV

S. No.	Course Type	Course Title	L	T	P	Credits
1	Dissertation	Dissertation Phase - II	--	--	32	16
		Total	**--**	**--**	**--**	**16**

Professional Elective -1

1. Embedded System Design
2. CMOS Analog Integrated Circuit Design
3. Advanced Microcontrollers
4. Advanced Operating Systems

Professional Elective -2

1. CMOS Digital Integrated Circuit Design
2. Digital Signal Processors and Architectures
3. TCP/IP and ATM Networks
4. Advanced Data Communication

Professional Elective -3

1. System on Chip Architectures
2. Embedded Software Engineering
3. Mixed Signal Design
4. Embedded Real Time Operating Systems

Professional Elective -4

1. Hardware and Software co-design
2. Low Power VLSI
3. Ad-hoc and Wireless Sensor Networks
4. Algorithms for VLSI Design

Professional Elective -5

1. Embedded Networks
2. Soft Computing Techniques
3. Communication Buses and Interfaces
4. VLSI Signal Processing

Open Elective

1. Principles of Signal Processing

DIGITAL SYSTEM DESIGN WITH PLDs

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Pre-Requisite: Switching Theory and Logic Design

Course Objectives

1) To provide extended knowledge of digital logic circuits in the form of state model approach.
2) To provide an overview of system design approach using programmable logic devices.
3) To provide and understand of fault models and test methods.
4) To get exposed to the various architectural features of CPLDS and FPGAS.
5) To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6) To expose software tools used for design process with the help of case studies.

Course Outcomes

1) To understands the minimization of Finite state machine.
2) To exposes the design approaches using ROM's, PAL's and PLA's.
3) To provide in depth understanding of Fault models.
4) To understands test pattern generation techniques for fault detection.
5) To design fault diagnosis in sequential circuits.
6) To provide exposure to various CPLDS and FPGAS available in market.
7) To acquire knowledge in one hot state machine design applicable to FPGA.
8) To get exposure to EDA tools.
9) To provide understanding in the design of flow using case studies.

UNIT I

Programmable Logic Devices

The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs- Altera CPLDs, FPGAs-FPGA technology, architecture, virtex CLB and slice- Stratix LAB and ALM-RAM Blocks, DSP Blocks, Clock Management, I/O standards, Additional features. [TEXTBOOK-1]

UNIT II

Analysis and derivation of clocked sequential circuits with state graphs and tables

A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. [TEXTBOOK-2]

UNIT III

Sequential circuit Design

Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]

UNIT IV

Fault Modeling and Test Pattern Generation

Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model. Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT V

Fault Diagnosis in sequential circuits

Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.1]

TEXTBOOKS

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth,Jr. -5th Ed.,Cengage Learning.
3. Logic Design Theory-N.N.Biswas,PHI.

REFERENCES

1. Digital Circuits and Logic Design-Samuel C.LEE,PHI, 2008.
2. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.

VLSI TECHNOLOGY AND DESIGN

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Pre-requisite: Switching Theory And Logic Design

Course Objectives

1) Students from other engineering background to get familiarize with large scale integration technology.
2) To expose fabrication methods, layout and design rules.
3) Learn methods to improve Digital VLSI system's performance.
4) To know about VLSI Design constraints.
5) Visualize CMOS Digital Chip Design.

Course Outcomes

1) Review of FET fundamentals for VLSI design.
2) To acquires knowledge about stick diagrams and layouts.
3) Enable to design the subsystems based on VLSI concepts.

UNIT I

Review of Microelectronics and Introduction to MOS Technologies-

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT II

Layout Design and Tools

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT III

Combinational Logic Networks

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT IV

Sequential Systems

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT V

Floor Planning

Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCES

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

EMBEDDED SYSTEMS DESIGN
(PE – 1)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Pre-Requisite: Microprocessor and Microcontrollers

Course Objectives
1. To differentiate between a General purpose and an Embedded System.
2. To provide knowledge on the building blocks of Embedded System.
3. To understand the requirement of Embedded firmware and its role in API.

Course Outcomes
1. Expected to differentiate the design requirements between General Purpose and Embedded Systems.
2. Expected to acquire the knowledge of firmware design principles.
3. Expected to understand the role of Real Time Operating System in Embedded Design.
4. To acquire the knowledge and experience of task level Communication in any Embedded System.

UNIT I
Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems,
Characteristics and Quality Attributes of Embedded Systems.

UNIT II
Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT III
Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT IV
RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT V
Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCES

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

CMOS ANALOG INTEGRATED CIRCUIT DESIGN
(PE – 1)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Pre-Requisite: Analog Electronics

Course Objectives

Analog circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology.

1. To understand most important building blocks of all CMOS analog Ics.
2. To study the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs.
3. To understand specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
4. To understand the design of differential amplifiers, current amplifiers and OP AMPs.

Course Outcomes

After studying the course, each student is expected to be able to

1. Design basic building blocks of CMOS analog ICs.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Determine the device dimensions of each MOSFETs involved.
4. Design various amplifiers like differential, current and operational amplifiers.

UNIT I

MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT II

Analog CMOS Sub-Circuits

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT III

CMOS Amplifiers

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT IV

CMOS Operational Amplifiers

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT V

Comparators

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCES

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

ADVANCED MICROCONTROLLERS
(PE -1)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: Microprocessors and Microcontrollers

Course Objectives

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.
3. Learn the programming on ARM Cortex M.

Course Outcomes

After completing this course the student will be able to:

1. To explore the selection criteria of ARM processors by understanding the functional level trade off issues.
2. Explore the ARM development towards the functional capabilities.
3. Expected to work with ASM level program using the instruction set.
4. Understand the architecture of ARM Cortex M and programming on it.

UNIT I

ARM Embedded Systems

RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals

Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors

Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT II

Introduction to the Arm Instruction Set

Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set

Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT III

Technical Details of ARM Cortex M Processors

General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT IV

Instruction SET of ARM Cortex M

Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT V

Floating Point Operations

About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

TEXTBOOKS

1. ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004.
2. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu, Elsevier Publications, 3rd Ed.,

REFERENCES

1. Arm System on Chip Architectures – Steve Furber, Edison Wesley, 2000.
2. ARM Architecture Reference Manual – David Seal, Edison Wesley, 2000.

ADVANCED OPERATING SYSTEMS
(PE -1)

M.Tech. I Year I-Sem

L	T	P	C
3	0	0	3

UNIT I
Introduction to Operating Systems
Overview of computer system hardware, Instruction execution, I/O function, |Interrupts, Memory hierarchy, I/O communication techniques, Operating system objectives and functions, Evaluation of operating system.

UNIT II
Introduction to UNIX and LINUX
Basic commands & command arguments, standard input, output, input / output redirection, filters and editors, Shells and operations.

UNIT III
System Calls
System calls and related file structures, input / output Process creation & termination.
Inter Process Communication
Introduction, file and record locking, Client-Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT IV
Introduction to Distributed Systems
Goals of distributed system, Hardware and software concepts, Design issues.
Communication in Distributed Systems
Layered protocols, ATM networks, Client – Server model, Remote procedure call and Group communicaton.

UNIT V
Synchronization in Distributed Systems
Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions.
Deadlocks
Deadlock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXTBOOKS

1. The Design of the UNIX Operating Systems – Maurice J. Bach, PHI, 1986.
2. Distributed Operating System – Andrew. S. Tanenbaum, PHI, 1994.
3. The Complete reference LINUX – Richard Peterson, 4th Ed., McGraw-Hill.

REFERENCES

1. Operating Systems: Internal and Design Principles – Stallings, 6th Ed., PE.
2. Modern operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles' – Abraham Silberchatz, peter B. Galvin, Greg Gagne,7th Ed., John Wiley.
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming – W. Richard Stevens, PHI, 1998.

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN
(PE - 2)

M.Tech. I Year I-Sem

L	T	P	C
3	0	0	3

UNIT I
MOS Design
Pseudo NMOS logic- Inverter, Inverter threshold voltage, output high voltage, Output low voltage, gain at gate threshold voltage, transient response, rise time, fall time, pseudo NMOS logic gates, transistor equivalency, CMOS inverter logic.

UNIT II
Combinational MOS logic circuits
MOS logic circuits with NMOS loads, Primitive CMOS logic gates- NOR and NAND gates, Complex logic circuits design- realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full-adder, cmos transmission gates, designing with transmission gates.

UNIT III
Sequential MOS logic circuits: Behavior of bistable elements, SR Latch, Clocked Latch and Flip-flop circuits, CMOS D Latch and edge triggered flip-flop.

UNIT IV
Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, high performance dynamic CMOS circuits.

UNIT V
Semiconductor Memories: Types, RAM array Organization, DRAM- types, operation, leakage currents in DRAM cell and refresh operation, SRAM - operation , leakage currents in SRAM cells, Flash memory- NOR flash and NAND flash.

TEXTBOOKS

1. Digital Integrated Circuit Design- Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuit Analysis and Design – Sung Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCES

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming Bo Lin, CRC Press, 2011.
2. Digital Integrated Circuits: A Designs Perspective - Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(PE -2)

M.Tech. I Year I-Sem **L T P C**
3 0 0 3

Pre-Requisite: Digital Signal Processing

Course Objectives
The main objectives of the course are:
1. To provide a comprehensive understanding of various programs of Digital Signal Processors.
2. To distinguish between the architectural differences of ARM and DSPs along with floating point capabilities.
3. To explore architecture and functionality of various DSP Processors and can able to write programs.
4. To known about the connectivity of interfacing devices with processors.

Course Outcomes
Upon completing this course, the student will be able to:
1. Understand the various processing operations on Digital signals.
2. Know the architecture of DSP Processors TMS320C54XX, ADSP 2100, 2181 and Blackfin Processor.
3. Run the programs on DSP Processors.
4. Interface Memory and I/O devices with DSP Processors.

UNIT –I
Fundamentals of Digital Signal Processing
Digital signal-processing system, Sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and Interpolation, Computational Accuracy in DSP Implementations-Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II
Architectures for Programmable DSP Devices
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III
Programmable Digital Signal Processors
Commercial Digital Signal-Processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX Processors.

UNIT –IV

Analog Devices Family of DSP Devices

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Blackfin Processor - The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals

UNIT –V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS

1. Digital Signal Processing: Principles, Algorithms & Applications – J.G. Proakis & D.G. Manolakis, 4th Ed., PHI,2006.
2. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.

REFERENCES

1. A Practical Approach to Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2009.
2. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, TMH, 2002.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al., S. Chand & Co. 2000.

TCP/IP AND ATM NETWORKS
(PE - 2)

M.Tech. I Year I-Sem **L T P C**
3 0 0 3

Prerequisite: Computer Networks

Course Objectives
The main objectives of the course are:
1. To study Network Layer Protocols, Next Generation IP protocols
2. To learn about User Datagram Protocol, Transmission Control Protocol and stream control Transmission protocol.
3. To understand techniques to improve QoS
4. To learn about Transport Layer Protocols for Ad Hoc Wireless Networks .
5. To study the features of ATM networks and various Interconnection Networks

Course Outcomes
At the end of the course, the student will be able to:
1. Get the concept of Network Layer Protocols and Transport Layer Protocols.
2. Understand and analyze about UDP, TCP AND SCTP protocols, flow and error control techniques.
3. Learn congestion control mechanisms and techniques to improve Quality of Service in switched networks
4. To understand the performance of TCP in Ad-hoc networks and various modified versions of TCP in ad-hoc networks
5. To understand features of Virtual circuit networks like ATM networks and their applications Design and analyze various types of Inter connection Networks,

UNIT I
Network Layer
Network Layer Services**,** Packet switching**,** , Network Layer Performance, IPv4 Addresses, Internet protocol(IP), ICMP v4, IPv6 Addressing, IPv6 protocol, ICMPv6 protocol, Transition from IPv4to IPv6,Mobile IP
Forwarding of IP Packets, Delivery- Direct Versus Indirect Delivery, Forwarding- Forwarding Techniques, Forwarding Process, Routing Table, Unicast routing- Routing algorithms, Unicast routing protocols, Multicast routing, Multicasting basics.

UNIT II
Transport Layer
Introduction to Transport Layer, Transport layer services, Connectionless Versus Connection Oriented Protocols, Transport Layer Protocols: Simple Protocols, Stop and Wait Protocols, Go Back N Protocol, Selective Repeat Protocol, Bidirectional Protocols: Piggybacking Transport layer protocols Services and Port Numbers.
UDP, TCP and SCTP
User Datagram Protocol (UDP)
User Datagram, UDP Services, UDP Applications
Transmission Control Protocol (TCP)

TCP Services, TCP Features, Segments, TCP Connection, State Transition Diagram, Windows in TCP, Flow and Error Control, TCP Timers,
SCTP: SCTP Services, SCTP Features, Packet Format, An SCTP Association SCTP Flow and Error Control

UNIT III
Traditional TCP
Congestion Control, Additive Increase Multiplicative Decrease (AIMD), Slow Start, Fast recovery, fast retransmit

TCP in Wireless Domain
Traditional TCP, TCP over wireless**,** Snoop TCP , TCP-Unaware Link Layer Indirect TCP, Mobile TCP, Explicit Loss Notification, WTCP, TCP SACK , Transaction-Oriented TCP

Transport Layer Protocols for Ad Hoc Wireless Networks
TCP Over Ad Hoc Wireless Networks- Feedback-Based TCP, TCP with Explicit Link Failure Notification, TCP-Bus, Ad Hoc TCP, Split TCP.

UNIT IV
Congestion Control and Quality of Service
Quality of Service- Flow Characteristics, Flow Classes, Techniques to Improve QoS-Scheduling, Traffic Shaping, Resource Reservation, Admission Control, Integrated Services-Signaling, Flow Specification, Admission, Service Classes, RSVP, Problems with Integrated Services , Differentiated Services.
Queue Management
Passive-Drop trial, Drop front, Random drop, Active- early Random drop, Random Early detection.

UNIT V
ATM Networks
ATM-Design Goals, Problems, Architecture, Switching, ATM Layers
SONET/SDH
Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks
Interconnection Networks
Introduction, Banyan Networks, Properties, Crossbar switch, Three stage Class Networks, Rearrangeable Networks, Folding algorithm, Benes Networks, Lopping algorithm, Bit allocation algorithm.

TEXT BOOKS

1. Data Communications and Networking - B. A.Forouzan, 5th edition, TMH, 2013.
2. Mobile Communications by Jochen H. Schiller, 2nd Edition, Pearson-Wesley, 2003.
3. Ad Hoc Wireless networks: Architectures and Protocols- C. Siva Ram Murthy and B. S.Manoj, PHI, 2004

REFERENCES

1. ATM Fundamentals –N.N Biswas, Adventure Books,1998
2. Data Communications and Computer Networks - Prakash C. Gupta, PHI, 2006.
3. Data and Computer Communications - William Stallings, 8th ed., PHI, 2007.

ADVANCED DATA COMMUNICATIONS
(PE - 2)

M.Tech. I Year I-Semester

L	T	P	C
0	0	4	2

Prerequisite: Digital Communication

Course Objectives

The main objectives of the course are:

1. To learn about basics of Data Communication networks, different protocols, standards and layering concepts.
2. To study about error detection and correction techniques.
3. To know about link layer, point to point, Medium Access and Control sub layer protocols.
4. To know about Switching circuits, Multiplexing and Spectrum Spreading techniques for data transmission.

Course Outcomes

At the end of the course, the student will be able to:

1. Understand the concepts of Networks and data link layer.
2. Acquire the knowledge of error detection, forward and reverse error correction techniques.
3. Compare the performance of different MAC protocols like Aloha, CSMA, CSMA/CA, TDMA, FDMA & CDMA.
4. Understand the significance of Switching circuits and characteristics of Wired LANs

UNIT I

Data Communications, Networks and Network Types, Internet History, Standards and Administration, Protocol Layering, TCP/IP protocol suite, OSI Model. Digital Data Transmission, DTE-DCE interface.

Data Link Layer

Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol.

UNIT II

Error Detection and Correction

Types of Errors, Redundancy, detection versus correction, Coding Block Coding: Error Detection, Vertical redundancy cheeks, longitudinal redundancy cheeks, Error Correction, Error correction single bit, Hamming code.

Cyclic Codes

Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum

Data Link Control: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol

UNIT III

Media Access Control (MAC) Sub Layer

Random Access, ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA),Controlled Access- Reservation, Polling- Token Passing,

Channelization - Frequency Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA).

Wired LANS

Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Giga bit Ethernet

UNIT IV

Switching

Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of switch

Multiplexing

Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing.

Spectrum Spreading

Spread Spectrum-Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum

Connecting devices

Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, Backbone Networks.

UNIT V

Networks Layer

Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic Host Configuration Protocol (DHCP), Network Address Resolution(NATF), Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches.

Unicast Routing

Introduction, Routing Algorithms-Distance Vector Routing, Link State Routing, Path Vector Routing, Unicast Routing Protocols- Routing Information Protocol(RIP), Open Short Path First .

TEXT BOOKS

1. Data Communications and Networking - B. A. Forouzan, 5th Ed., TMH, 2013.
2. Data and Computer Communications - William Stallings, 8th Ed., PHI, 2007.

REFERENCES

1. Data Communications and Computer Networks - Prakash C. Gupta, PHI, 2006.
2. Data Communications and Networking - B. A. Forouzan, 2nd Ed., TMH, 2013.
3. Data Communications and Computer Networks- Brijendra Singh, 2nd Ed., 2008.

DIGITAL SYSTEM DESIGN LABORATORY

M.Tech. I Year I-Semester

L	T	P	C
0	0	4	2

I. Student has to design his/her user defined library components by using and standard HDL simulator and Synthesis tool for target FPGA device.

II. Combinational Logic Circuits

- Generic Multiplexer.
- Generic Priority Encoder.
- Design of RAM Memory.
- Code Converters.

Combinational Arithmetic circuits

- Ripple Carry Adder.
- Carry-Look ahead adder.
- Signed and Unsigned Adders.
- Signed and Unsigned Subtractors.
- N-bit Comparator.
- N – bit Arithmetic Logic Unit.
- Parallel Signed and unsigned Multipliers.
- Dividers.

III. Sequential Circuits

- Shift Register with Load.
- Switch Debouncer.
- Timer.
- Fibonacci Series Generator.
- Frequency Meters.

- Student has to design his/her user Library consisting of following circuits / components. (use any Standard HDL simulator and synthesis tool for a target FPGA device available in Lab.)

The library components required

1. Adders, Subtractors, Multiplexers, Decoders, Encoders, code converters, n-bit adders – Ripple Carry adders, carry – look ahead adder, n-bit comparator, n-bit ALU, Multipliers, MAC units.
2. Different Latches & Flip-flops, shift Registers, Converters, Sequence generators, Sequence detector, 2D-memory devices, clock generators, clock dividers, e.t.c
3. At the end each student has to design an application hardware using these components in library.

SCRIPTING LANGUAGES LABORATORY

M.Tech. I Year II-Semester

L	T	P	C
0	0	4	2

Prerequisites: Students should install Python on Linux platform.

List of Programs

Part: I
Preliminary Exercises:

1. To demonstrate different number data types in Python.
2. To perform different Arithmetic Operations on numbers in Python.
3. To create, concatenate and print a string and accessing sub-string from a given string.
4. Write a python script to print the current date in the following format "Sun May 29 02:26:23 IST 2017"
5. To demonstrate working with dictionaries in python.
6. To find largest of three numbers.
7. Write a Python program to construct the a pattern, using a nested for loop.
8. Write a Python script that prints prime numbers less than 20.
9. To convert temperatures to and from Celsius, Fahrenheit.

Part: II

10. To create, append, and remove lists in python.
11. To demonstrate working with tuples in python.
12. To find factorial of a number using Recursion.
13. Write a Python class to implement pow(x, n)
14. Write a script named copyfile.py. This script should prompt the user for the names of two text files. The contents of the first file should be input and written to the second file.
15. Write a program that inputs a text file. The program should print all of the unique words in the file in alphabetical order.
16. Write a Python class to find the frequency of each alphabet (of any language) in the given text document.

RESEARCH METHODOLOGY AND IPR

M.Tech. I Year II-Semester

L	T	P	C
2	0	0	2

Course Objectives

1. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
2. Follow research related information
3. Understanding that when IPR would take such important place in growth of individuals and nation, it is needless to emphasis the need of information about intellectual Property Right to be promoted among students in general & engineering in particular.
4. Understand that IPR protection leads to economic growth and social benefits

Course Outcomes

At the end of this course, students will be able to:

1. Understand research problem formulation.
2. Analyze research problem formulation.
3. Understand the IPR protection provides incentive top inverters for further research work and investment in R & D.
4. Understand that IPR protection leads to creation of new and better products.

UNIT I

Meaning of research problem, sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem, approaches of investigation of solutions for research problem.

UNIT II

Data collection, analysis, interpretation, necessary instrumentations, Effective literature studies approaches, analysis Plagiarism, and Research ethics

UNIT III

Effective technical writing, how to write report, paper, Developing a research proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT IV

Nature of Intellectual property

Patents, Designs, Trade, Copyright, copy left, copy right, creative commence, Process of Patenting and Development - technological research, innovation, patenting, development. International Scenario- International cooperation on intellectual property, Procedure for grants of patents, Patenting under PCT.

UNIT V

Patents Rights

Scope of Patents Rights, Licensing and transfer of technology, Patents information and databases, Geographical Indications, Administration of Patent System, New developments in IPR - IPR of Biological Systems, Computer Software etc., Traditional Knowledge Case Studies.

REFERENCES

- Stuart Melville and Wayne Goddard, " Research methodology: An introduction for science & engineering students"
- Wayne Goddard and Stuart Melville, " Research methodology: An introduction"
- Ranjit Kumar, 2ND Edition, " Research methodology: A Step by Step Guide for beginners"
- Halbert, " Resisting Intellectual Property", Taylor & Francis Ltd, 2007.
- Mayall, " Industrial Design", McGraw Hill, 1992.
- Niebel, " Product Design", McgRAW Hill, 1974.
- Asimov, " Introduction to Design", Prentice Hall, 1962.
- Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age". 2016.
- T. Ramappa, " Intellectual Property Rights Under WTO", S. Chand, 2008

ADVANCED COMPUTER ARCHITECTURES

M.Tech. I Year II-Sem

L	T	P	C
3	0	0	3

Pre-Requisite: Computer Organization and Operating Systems.

Course Objectives

1. Explains instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
2. Explains different classifications of instruction set architectures.
3. Explains the advanced concepts such as instruction level parallelism, , out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction.
4. Examine software support for ILP, including VLIW and similar approaches.
5. Teach memory hierarchy design issues, including caching and virtual memory approaches.
6. Explains multiprocessor and parallel processing architectures.
7. Gives the organization and design of contemporary processor architectures.
8. As the current trend in computer architecture is towards chip-multiprocessing, the architecture of shared memory multiprocessors and chip level interconnect (network-on-chip) will be covered as future scope.

Course Outcomes

A student who has met the objectives of the course will be able to

1. Understand advanced computer architecture aspects.
2. Describe and explain instruction level parallelism with static scheduling, out-of-order execution and network-on-chip architectures.
3. Understand the architecture and limitations of chip-multiprocessing.
4. Explain in detail about time-predictable computer architecture.
5. Understand the operation of modern CPUs including pipelining, memory systems and busses.
6. Design and emulate a single cycle or pipelined CPU by given specifications using Hardware Description Language (HDL).
7. Write reports and make presentations of computer architecture projects.

UNIT I

Fundamentals of Computer Design

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT II

Pipelines

Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design

Introduction, review of ABC of cache, Cache performance , Reducing cache miss penalty, Virtual memory.

UNIT III

Instruction Level Parallelism the Hardware Approach

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach

Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT IV

Multi Processors and Thread Level Parallelism

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT V

Inter Connection and Networks

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture

Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS

1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.

REFERENCES

1. John P. Shen and Miikko H. Lipasti, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs., MC Graw Hill.,
3. Advanced Computer Architecture - A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk ,Pearson Ed.,

DESIGN OF FAULT TOLERANT SYSTEMS

M.Tech. I Year II-Sem

L	T	P	C
3	0	0	3

Pre-Requisite: Digital System Design with PLDs

Course Objectives

1) To provide broad understanding of fault diagnosis and tolerant design approach.
2) To illustrate the framework of test pattern generation using semi and full automatic approach.

Course Outcomes

1) To acquire the knowledge of fundamental concepts in fault tolerant design.
2) To acquire the knowledge of design requirements of self check-in circuits.
3) To acquire the knowledge of test pattern generation using LFSR.
4) To acquire the knowledge of design for testability rules and techniques for combinational circuits.
5) To acquire the knowledge of scan architectures.
6) To acquire the knowledge of design of built-in-self test.

UNIT I

Fault Tolerant Design

Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.

Fault Tolerant Design

Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts. [TEXTBOOK-1]

UNIT II

Self Checking circuits & Fail safe Design

Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

Fail Safe Design- Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design. [TEXTBOOK-1]

UNIT III

Design for Testability

Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.

Design for testability by means of scan

Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.[TEXTBOOK-2]

UNIT IV

Logic Built-in-self-test

BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralised and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results. [TEXTBOOK-2]

UNIT V

Standard IEEE Test Access Methods

Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language. [TEXTBOOK-2]

TEXTBOOKS

1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala,PHI, 1984.
2. Digital System Test and Testable Design using HDL models and Architectures -Zainalabedin Navabi, Springer International Ed.,

REFERENCES

1. Digital Systems Testing and Testable Design-Miron Abramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books
2. Essentials of Electronic Testing- Bushnell & Vishwani D.Agarwal,Springers.
3. Design for Test for Digital IC's and Embedded Core Systems- Alfred L. Crouch, 2008

SYSTEM ON CHIP ARCHITECTURES
(PE - 3)

M.Tech. I Year III-Sem

L	T	P	C
3	0	0	3

Pre-Requisite: Embedded System Design

Course Objectives
1) To introduce the architectural features of system on chip.
2) To imbibe the knowledge of customization using case studies.

Course Outcomes
1) Expected to understand SOC Architectural features.
2) To acquire the knowledge on processor selection criteria and limitations
3) To acquires the knowledge of memory architectures on SOC.
4) To understands the interconnection strategies and their customization on SOC.

UNIT I
Introduction to the System Approach
System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT II
Processors
Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III
Memory Design for SOC
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I , and D – Caches , Multilevel Caches, Virtual to real translation , SOC Memory System , Models of Simple Processor – memory interaction.

UNIT IV
Interconnect Customization and Configuration
Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V
Application Studies / Case Studies

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JEPG compression.

TEXT BOOKS

1. Computer System Design System-on-Chip by Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Eed., 2000, Addison Wesley Professional.

REFERENCES

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., Springer,2004.
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, Kluwer Academic Publishers,2001.

EMBEDDED SOFTWARE ENGINEERING
(PE – 3)

M.Tech. I Year II-Sem

L	T	P	C
3	0	0	3

UNIT I

Software Engineering of Embedded and Real-Time Systems

Software engineering, Embedded systems, Embedded systems are reactive systems, Real-time systems, Soft and Hard Real-Time systems, Efficient execution and the execution environment, Resource management, Challenges in real-time system design.

UNIT II

The embedded system software build process, Distributed and multi-processor architectures, Software for embedded systems, Super loop architecture, Power-save super loop, Window lift embedded design, Hardware abstraction layers (HAL) for embedded systems, HW/SW prototyping, Industry design chain, Different types of virtual prototypes, Architecture virtual prototypes, Software virtual prototypes.

UNIT III

Events, Triggers and Hardware Interface to Embedded Software

Events and triggers, Event system, Event handle, Event methods, Event data structure, Reentrancy, Disable and enable interrupts, Semaphores, Implementation with Enter/ExitCritical, Event processing, Integration, Triggers, Blinking LED, Design idea, Tick timer, Trigger interface, Trigger descriptor, Data allocation, SetTrigger, IncTicks, Making it reentrant, Initialization, Real-time aspects, Introduction to Hardware Interface, Collaboration, System integration, Launching tasks in hardware, Debug hooks, Compile-time switches, Build-time switches, Run-time switches, Self-adapting switches, Difficult hardware interactions, Testing and troubleshooting.

UNIT IV

Embedded Software Programming and Operating Systems

Introduction, Principles of high-quality programming, Readability, Maintainability, Testability, Starting the embedded software project, Libraries from third parties, Team programming guidelines, Syntax standard, Conditional compilation, Foreground/background systems, Real-time kernels, RTOS (real-time operating system), Critical sections, Task management, Preemptive scheduling, Context switching, Interrupt management, Non-kernel-aware interrupt service routine (ISR), Processors with multiple interrupt priorities, The clock tick (or system tick), Wait lists, Time management, Resource management, Synchronization, Message passing, Flow control,
Clients and servers, Memory management

UNIT V

Software Reuse and Performance Engineering in Embedded Systems

Kinds of software reuse, Implementing reuse by layers,Arbitrary extensibility, Ebedded Software for Performance, The code optimization process, Using the development tools, Compiler optimization

TEXTBOOKS

1. Software Engineering for Embedded Systems: Methods, Practical Techniques, and Applications, by Oshana, Robert; Kraeling, Mark, “Newnes” Publishers, 2013.

MIXED SIGNAL DESIGN
(PE – 3)

M.Tech. I Year II-Sem

L	T	P	C
3	0	0	3

Pre-Requisite Analog Electronics

Course Objectives
The objectives of this course are to

1. Introduce circuit design concepts for basic building blocks used in mixed-signal integrated circuit designs.
2. Provide students with the skills to design mixed-signal integrated circuits with these building blocks.
3. Understand design and operation of basic analog circuits.
4. Know mixed signal circuits like DAC, ADC, PLL etc.
5. Design and analysis of switched capacitor circuits
6. Analysis basic data conversion algorithms and circuits.

Course Outcomes

At the completion of this course, each student will have demonstrated proficiency in:

1. Designing CMOS analog circuits to achieve performance specifications.
2. Analyzing CMOS based switched capacitor circuits.
3. Understanding basics of data converters.
4. Understanding mixed-signal design flow.

UNIT I

Switched Capacitor Circuits

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT II

Phased Lock Loop (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT III

Data Converter Fundamentals

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT IV

Nyquist Rate A/D Converters

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT V

Oversampling Converters

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.

TEXT BOOKS

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013.

REFERENCES

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

EMBEDDED REAL TIME OPERATING SYSTEMS
(PE – 3)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Pre-Requisite: Computer Organization and Operating Systems.

Course Objectives

1. To provide broad understanding of the requirements of Real Time Operating Systems.

2. To make the student understand, applications of these Real Time features using case studies.

Course Outcomes

1. To acquire knowledge on Real Time features of UNIX and LINUX.
2. To understand the basic building blocks of Real Time Operating Systems in terms of scheduling , context switching and ISR.
3. Elaborative understanding on Real Time applications using Real Time Linux, ucos2, VX works, Embedded Linux, e.t.c.

UNIT I

Introduction

Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT II

Real Time Operating Systems

Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.

Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.

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UNIT III

Objects, Services and I/O

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

UNIT IV

Exceptions, Interrupts and Timers

Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT V Case Studies of RTOS

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOKS

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.

REFERENCES

1. Embedded Systems- Architecture, Programming and Design by Rajkamal,TMH, 2007.
2. Advanced UNIX Programming, Richard Stevens.
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh.

HARDWARE AND SOFTWARE CO-DESIGN
(PE – 4)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Pre-Requisite: Advanced Computer architecture , Embedded System Design.

Course Objective

1. To provide a broad understanding of the specific requirement of Hardware and soft ware integration for embedded system.
2. To emphasize on the design specifications and tools in the Hardware – Software Co-design.

Course Outcomes

1. To acquire the knowledge on various models of Co-design.
2. To explore the interrelationship between Hardware and software in a embedded system
3. To acquire the knowledge of firmware development process and tools during Co-design.
4. Understand validation methods and adaptability.

UNIT I

Co- Design Issues

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co-Synthesis Algorithms**

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT II

Prototyping and Emulation

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III

Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT IV

Design Specification and Verification

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT V

Languages for System – Level Specification and Design-I

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami,Kluwer Academic Publishers, 2002.

REFERENCES

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer, 2010.

LOW POWER VLSI
(PE – 4)

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Pre-Requisite: VLSI

Course Objectives

The objectives of this course are to:

1. Identify sources of power in an IC.
2. Identify the power reduction techniques based on technology independent and technology dependent Power dissipation mechanism in various MOS logic style.
3. Identify suitable techniques to reduce the power dissipation.
4. Design adders, Multipliers and memory circuits with low power dissipation.

Course Outcomes

1. The student will get to know the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays major role.
2. The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

UNIT I

Fundamentals

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II

Low-Power Design Approaches

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches

System Level Measures, Circuit Level Measures, Mask level Measures.

UNITIII Low-Voltage Low-Power Adders

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT IV

Low-Voltage Low-Power Multipliers

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT V

Low-Voltage Low-Power Memories

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCES

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.

AD-HOC AND WIRELESS SENSOR NETWORKS
(PE- 4)

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: Wireless Sensor Networks

Course Objectives

The objectives of this course are to make the student
1. To study the fundamentals of wireless Ad-Hoc Networks.
2. To study the operation and performance of various Adhoc wireless network protocols.
3. To study the architecture and protocols of Wireless sensor networks.

Course Outcomes

On completion of this course student will be able to
1. Students will be able to understand the basis of Ad-hoc wireless networks.
2. Students will be able to understand design, operation and the performance of MAC layer protocols of Adhoc wireless networks.
3. Students will be able to understand design, operation and the performance of routing protocol of Adhoc wireless network.
4. Students will be able to understand design, operation and the performance of transport layer protocol of Adhoc wireless networks.
5. Students will be able to understand sensor network Architecture and will be able to distinguish between protocols used in Adhoc wireless network and wireless sensor networks.

UNIT - I
Wireless LANs and PANs: Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.
AD HOC WIRELESS NETWORKS: Introduction, Issues in Ad Hoc Wireless Networks.

UNIT - II
MAC Protocols: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT - III
Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT – IV
Transport Layer Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless

Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT – V

Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

TEXT BOOKS

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.

REFERENCES

1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C.K. Toh , 1st Ed. Pearson Education.
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer

ALGORITHMS FOR VLSI DESIGN
(PE - 4)

M.Tech. I Year II-Sem

L	T	P	C
4	0	0	4

Pre-Requisite: VLSI

Course Objectives

The objectives of this course are to:
1. To provide knowledge on broad spectrum of issues related to design automation of VLSI circuits.
2. To provide exposure to various tools and their applications in design automation.

Course Outcomes
On completion of this course the student will be able to:
1. Expected to learn graph theory and its applications.
2. To understand the methods of combinational circuit optimization.
3. To learn optimization approaches in synthesis and verification.
4. To expose design automation using FPGA.
5. To study elaborately on physical design automation.

UNIT I
PRELIMINARIES
Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION
Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III
LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING
Problems, Concepts and Algorithms. MODELLING AND SIMULATION
Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT IV
LOGIC SYNTHESIS AND VERIFICATION
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis
HIGH-LEVEL SYNTHESIS, Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V
PHYSICAL DESIGN AUTOMATION OF FPGAs
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs

MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.1999.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed.,Springer International Edition, 2005.

REFERENCES

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson,Wiley, 1993.
2. Modern VLSI Design :Systems on silicon – Wayne Wolf, 2nd Ed., Pearson Education Asia, 1998.

EMBEDDED SYSTEMS LABORATORY

M.Tech. I Year II-Sem

L	T	P	C
0	0	4	2

List of Experiments

1. **Functional Testing Of Devices**
   Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems**
   Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming**
   Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430**
   Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity**
   Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. **Battery Voltage Range Indicator**
   Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V).
7. **Dice Game Simulation**
   Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface**
   Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Openwrt To the Device**
   Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board**

Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server(eg: Apache) and thereby host the website.

11. **Webcam Server**
    Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission**
    Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz).

Note : Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

SIMULATION LABORATORY

M.Tech. I Year II-Semester

L	T	P	C
0	0	4	2

List of Experiments

1. Overview of EDA Tools Micro Wind / Cadence / Electric
2. Dynamic Charecteristics of CMOS Inverter
3. Design and Simulation of Combinational Circuits
4. Design and Simulation of Sequential Circuits
5. Design and Simulation of Source Follower Circuits
6. Design and Simulation of Cascode Amplifier
7. Design and Simulation of Current Mirror Amplifier
8. Design and Simulation of Differential Amplifier

EMBEDDED NETWORKS
(PE – 5)

M.Tech. I Year III-Semester

L	T	P	C
3	0	0	3

Pre-Requisite Computer Networks

Course Objectives
1. To through the light on the requirements of Embedded Networks.
2. Understanding the role of various protocols in wired and wireless Embedded Networks.

Course Outcomes
On completion of this course the student will be able to:
1. To make the students understand various Embedded Network protocols.
2. Acquires the knowledge of CAN bus design requirements.
3. To make the student aware of Ethernet design principles while building an Embedded Network.
4. To acquire the knowledge on the conceptual framework of Wireless Sensor Networks and their design requirements.

UNIT I
Embedded Communication Protocols
Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT II
USB and CAN Bus
USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors – Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT III
Ethernet Basics
Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –

Using the internet in local and internet communications – Inside the Internet protocol.

UNIT IV

Embedded Ethernet

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT V

Wireless Embedded Networking

Wireless sensor networks – Introduction – Applications – Network Topology – Localization – Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002.
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCES

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari□, Cambridge press 2005.

SOFT COMPUTING TECHNIQUES
(PE - 5)

M.Tech. I Year III-Sem

L	T	P	C
3	0	0	3

UNIT I

Fundamentals of Neural Networks & Feed Forward Networks

Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT II

Associative Memories & ART Neural Networks

Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT III

Fuzzy Logic & Systems

Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT IV

Genetic Algorithms

Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

UNIT V

Hybrid Systems

Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

TEXT BOOKS

1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2. Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications - S.Rajasekaran, G.A. Vijayalakshmi Pai, PHI, New Delhi, July 2011.
3. Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.
4. Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.

REFERENCES

1. Artificial Neural Networks - Dr. B. Yagananarayana, PHI, New Delhi, , 1999.
2. An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998
3. Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.

COMMUNICATION BUSES AND INTERFACES
(PE-5)

M.Tech. I Year III-Semester

L	T	P	C
3	0	0	3

UNIT I

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features

Limitations and applications of RS232, RS485, I^2C , SPI

UNIT II

CAN

ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

UNIT III

PCIe

Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT IV

USB

Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

UNIT V

Data streaming Serial Communication Protocal- Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

TEXTBOOKS

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.,

REFERENCES

1. USB Complete – Jan Axelson, Penram Publications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

VLSI SIGNAL PROCESSING
(PE-5)

M.Tech. I Year III-Sem

L	T	P	C
3	0	0	3

Prerequisite: VLSI Technology, Digital Signal Processing

Course Objectives

The objectives of this course are to:

1. Introduce techniques for the existing DSP structures to suit VLSI implementations.
2. Introduce efficient design of DSP architectures suitable for VLSI.
3. Understand various fast convolution techniques.
4. Understand low power processors for signal processing and wireless applications

Course Outcomes

On successful completion of the module, students will be able to:

1. Ability to modify the existing or new DSP architectures suitable for VLSI.
2. Understand the concepts of folding and unfolding algorithms and applications.
3. Ability to implement fast convolution algorithms.
4. Low power design aspects of processors for signal processing and wireless applications.

UNIT -I

Introduction to DSP

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

Pipelining and Parallel Processing

Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power

Retiming

Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT –II

Folding and Unfolding

Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems

Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT -III

Systolic Architecture Design

Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT -IV

Fast Convolution

Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT -V

Low Power Design

Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Programmable DSP

Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parthi, Wiley Inter Science, 1998.
2. VLSI and Modern Signal processing – Kung S. Y, H. J. While House, T. Kailath, Prentice Hall, 1985.

REFERENCES

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
2. VLSI Digital Signal Processing – Medisetti V. K, IEEE Press (NY), 1995.

PRINCIPLES OF SIGNAL PROCESSING
(OE)

M.Tech. I Year III-Sem

L	T	P	C
3	0	0	3

Course Objectives

1. This gives the basics of Signals and Systems required for all Engineering related courses.
2. To understand the basic characteristics of LTI systems.
3. To know the signal transmission requirements.
4. This gives basic understanding of signal statistical properties and noise source concepts.

Course Outcomes

Upon completing this course, the student will be able to

1. Differentiate various signal functions.
2. Understand the characteristics of linear time invariant systems.
3. Understand the concepts sampling theorem.
4. Determine the Spectral and temporal characteristics of Signals.
5. Understand the concepts of Noise in Communication systems.

UNIT I

Signal Analysis

Analogy between Vectors and Signals, Orthogonal Signal Space, Signal approximation using Orthogonal functions, Mean Square Error, Closed or complete set of Orthogonal functions, Orthogonality in Complex functions, Classification of Signals and systems, Exponential and Sinusoidal signals, Concepts of Impulse function, Unit Step function, Signum function.

UNIT II

Signal Transmission through Linear Systems

Linear System, Impulse response, Response of a Linear System, Linear Time Invariant(LTI) System, Linear Time Variant (LTV) System, Transfer function of a LTI System, Filter characteristic of Linear System, Distortion less transmission through a system, Signal bandwidth, System Bandwidth, Ideal LPF, HPF, and BPF characteristics, Convolution and Correlation of Signals, Concept of convolution in Time domain and Frequency domain, Graphical representation of Convolution.

UNIT III

Sampling Theorem

Graphical and analytical proof for Band Limited Signals, Impulse Sampling, Natural and Flat top Sampling, Reconstruction of signal from its samples, Effect of under sampling – Aliasing, Introduction to Band Pass Sampling.

UNIT IV

Temporal characteristics of signals

Concept of Stationarity and Statistical Independence. First-Order Stationary Processes, Time Averages and Ergodicity, Cross Correlation and Auto Correlation of Functions, Properties of Correlation Functions, Cross-Correlation Function and Its Properties. Power Spectrum and its Properties, Relationship between Power Spectrum and Autocorrelation Function.

UNIT V

Noise sources

Resistive/Thermal Noise Source, Arbitrary Noise Sources, Effective Noise Temperature, Noise equivalent bandwidth, Average Noise Figures, Average Noise Figure of cascaded networks, Narrow Band noise, Quadrature representation of narrow band noise & its properties.

TEXT BOOKS

1. Signals, Systems & Communications - B.P. Lathi , B.S. Publications, 2013.
2. Probability, Random Variables & Random Signal Principles - Peyton Z. Peebles, TMH, 4th Edition, 2001.

REFERENCES

1. Signals and Systems - A.V. Oppenheim, A.S. Willsky and S.H. Nawabi, 2 Ed.
2. Fundamentals of Signals and Systems - Michel J. Robert, 2008, MGH International Edition.
3. Random Processes for Engineers-Bruce Hajck, Cambridge unipress,2015
4. Statistical Theory of Communication – S.P Eugene Xavier, New Age Publications, 2003.