

**JNTUH COLLEGE OF ENGINEERING HYDERABAD
(AUTONOMOUS)
M.Tech. (Embedded Systems) – Full Time w.e.f. 2018-19**

SEMESTER – I

S. No.	Course Type	Course Title	L	T	P	Credits
1	Core 1	Embedded System Design	3	0	0	3
2	Core 2	Digital Control Systems	3	0	0	3
3	P E - 1	Professional Elective 1	3	0	0	3
4	P E - 2	Professional Elective 2	3	0	0	3
5	Lab 1	Embedded System Lab	0	0	4	2
6	Lab 2	Simulation Lab	0	0	4	2
7		Research Methodology and IPR	2	0	0	2
8	Aud 1	Audit Course 1	2	0	0	0
		Total	16	0	8	18

SEMESTER – II

S. No.	Course Type	Course Title	L	T	P	Credits
1	Core 3	System on Chip Architectures	3	0	0	3
2	Core 4	Embedded Programming	3	0	0	3
3	P E – 3	Professional Elective 3	3	0	0	3
4	P E – 4	Professional Elective 4	3	0	0	3
5	Lab 3	Embedded Programming Lab	0	0	4	2
6	Lab 4	Scripting Languages Lab	0	0	4	2
7		Mini Project with Seminar	0	0	4	2
8	Aud 2	Audit Course 2	2	0	0	0
		Total	16	0	8	18

SEMESTER - III

S. No.	Course Type	Course Title	L	T	P	Credits
1	P E – 5	Professional Elective 5	3	0	0	3
2	O E	Open Elective	3	0	0	3
3	Dissertation	Dissertation Phase - I	0	0	20	10
		Total	06	0	20	16

SEMESTER - IV

S. No.	Course Type	Course Title	L	T	P	Credits
1	Dissertation	Dissertation Phase - II	--	--	32	16
		Total	--	--	--	16

Professional Elective 1

1. Digital Systems Design with PLDs
2. VLSI Technology and Design
3. Advanced Microcontrollers
4. CMOS Digital Integrated Circuit Design

Professional Elective 2

1. High Performance Networks
2. Mobile Computing
3. Artificial Intelligence
4. Advanced Computer Networks

Professional Elective 3

1. Reliability Engineering
2. Intelligent Control
3. Sensors and Actuators
4. Modern Control Theory

Professional Elective 4

1. Design of Fault Tolerant Systems
2. Embedded Software Engineering
3. Embedded Real Time Operating Systems
4. Hardware and Software co-design

Professional Elective 5

1. Embedded Networks
2. Communication Buses and Interfaces
3. Robotics
4. Soft Computing Techniques

EMBEDDED SYSTEMS DESIGN

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: Microprocessor and Microcontrollers

Course Objectives

1. To provide an overview of Design Principles of Embedded System.
2. To provide clear understanding about the role of firmware , operating systems in correlation with hardware systems.

Course Outcomes

1. Expected to understand the selection procedure of Processors in the Embedded domain.
2. Design Procedure for Embedded Firmware.
3. Expected to visualize the role of Real time Operating Systems in Embedded Systems
4. Expected to evaluate the Correlation between task synchronization and latency issues

UNIT I

Introduction to Embedded Systems

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT II

Typical Embedded System

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT III

Embedded Firmware

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT IV

RTOS Based Embedded System Design

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT V

Task Communication

Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXTBOOKS

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCES

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

DIGITAL CONTROL SYSTEMS

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: Control Systems

Course Objectives

1. To explain basic and digital control system for the real time analysis and design of control systems.
2. To apply the knowledge state variable analysis in the design of discrete systems.
3. To explain the concept of stability analysis and design of discrete time systems.

Course Outcomes

Upon the completion of this course, the student will be able to

1. Apply the concepts of Digital control systems.
2. Analyze and design of discrete systems in state variable analysis.
3. To relate the concepts of stability analysis and design of discrete time systems.

UNIT I

Concept & Representation of Discrete time Systems

Block Diagram of typical control system- advantages of sampling in control systems – examples of discrete data and digital systems – data conversion and quantization – sample and hold devices – D/A and A/D conversion – sampling theorem – reconstruction of sampled signals.

Z-transform

Definition of Z-transforms – mapping between s-plane and z-plane – inverse z- transform – properties of z-transforms - ROC of z-transforms –pulse transfer function –relation between $G(s)$ and $G(z)$ – signal flow graph method applied to digital control systems.

UNIT II

STATE SPACE ANALYSIS

State space modeling of discrete time systems – state transition equation of discrete time invariant systems – solution of time invariant discrete state equations: recursive method and the Z-Transformation method – conversion of pulse transfer function to the state model & vice-versa – Eigen values – Eigen vectors of discrete time system-matrix (A) – Realization of pulse transformation in state space form, discretization of continuous time systems, Computation of state transition matrix and its properties. Response of sample data system between sampling instants.

UNIT III

Controllability, Observability & Stability tests

Concept of controllability, stabilizability, observability and reachability - Controllability and observability tests, Transformation of discrete time systems into controllable and observable forms.

Stability

Definition of stability – stability tests – The second method of Liapunov.

UNIT IV

Design of discrete time Controllers and observers

Design of discrete time controller with bilinear transformation – Realization of digital PID controller- Design of deadbeat controller; Pole placement through state feedback.

UNIT V

STATE OBSERVERS

Design of - Full order and reduced order observers. Study of observer based control design

TEXTBOOKS

1. K. Ogata , Discrete-Time Control systems, Pearson Education/PHI, 2nd Edition.
2. V. I. George, C. P. Kurian, Digital Control Systems, Cengage Learning.
3. M.Gopal, Digital Control Engineering, New Age Int. Pvt. Ltd., 2014

REFERENCES

1. Kuo, Digital Control Systems, Oxford University Press, 2nd Edition, 2003.
2. M.Gopal , Digital Control and State Variable Methods, TMH.
3. M. Sami Fadali Antonio Visioli, Digital Control Engineering Analysis and Design, Academic Press

**DIGITAL SYSTEM DESIGN WITH PLDs
(PE-1)**

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: Switching Theory and Logic Design

Course Objectives

- 1 To provide extended knowledge of digital logic circuits in the form of state model approach.
- 2 To provide an overview of system design approach using programmable logic devices.
- 3 To provide and understand of fault models and test methods.
- 4 To get exposed to the various architectural features of CPLDs and FPGAs.
- 5 To learn the methods and techniques of CPLD & FPGA design with EDA tools.
- 6 To expose software tools used for design process with the help of case studies.

Course Outcomes

- 1 To understands the minimization of Finite state machine.
- 2 To exposes the design approaches using ROM's, PAL's and PLA's.
- 3 To provide in depth understanding of Fault models.
- 4 To understands test pattern generation techniques for fault detection.
- 5 To design fault diagnosis in sequential circuits.
- 6 To provide exposure to various CPLDs and FPGAs available in market.
- 7 To acquire knowledge in one hot state machine design applicable to FPGA.
- 8 To get exposure to EDA tools.
- 9 To provide understanding in the design of flow using case studies.

UNIT I

Programmable Logic Devices

The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs- Altera CPLDs, FPGAs-FPGA technology, architecture, virtex CLB and slice- Stratix LAB and ALM-RAM Blocks, DSP Blocks, Clock Management, I/O standards, Additional features. [TEXTBOOK-1]

UNIT II

Analysis and derivation of clocked sequential circuits with state graphs and tables

A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. [TEXTBOOK-2]

UNIT III

Sequential circuit Design

Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]

UNIT IV

Fault Modeling and Test Pattern Generation

Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.

Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT V

Fault Diagnosis in sequential circuits

Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.1]

TEXTBOOKS

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth,Jr. -5th Ed.,Cengage Learning.
3. Logic Design Theory-N.N.Biswas,PHI

REFERENCES

1. Digital Circuits and Logic Design-Samuel C.LEE,PHI 2008
2. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.

**VLSI TECHNOLOGY AND DESIGN
(PE-1)**

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: VLSI , ICA

Course Objectives

1. Students from other engineering background to get familiarize with large scale integration technology.
2. To expose fabrication methods, layout and design rules.
3. Learn methods to improve Digital VLSI system's performance.
4. To know about VLSI Design constraints.
5. Visualize CMOS Digital Chip Design.

Course Outcomes

1. Review of FET fundamentals for VLSI design.
2. To acquires knowledge about stick diagrams and layouts.
3. Enable to design the subsystems based on VLSI concepts.

UNIT I

Review of Microelectronics and Introduction to MOS Technologies

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: $I_{ds} - V_{ds}$ relationships, Threshold Voltage V_T , G_m , G_{ds} and ω_o , Pass Transistor, MOS, CMOS & BiCMOS Inverters, Z_{pu}/Z_{pd} , MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT II

Layout Design and Tools

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT III

Combinational Logic Networks

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT IV

Sequential Systems

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT V

Floor Planning

Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXTBOOKS

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCES

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

**ADVANCED MICROCONTROLLERS
(PE -1)**

M.Tech. I Year I-Semester

**L T P C
3 0 0 3**

Prerequisite: Microprocessors and Microcontrollers

Course Objectives

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.
3. Learn the programming on ARM Cortex M.

Course Outcomes

After completing this course the student will be able to:

1. To explore the selection criteria of ARM processors by understanding the functional level trade off issues.
2. Explore the ARM development towards the functional capabilities.
3. Expected to work with ASM level program using the instruction set.
4. Understand the architecture of ARM Cortex M and programming on it.

UNIT I

ARM Embedded Systems

RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals

Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors

Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT II

Introduction to the Arm Instruction Set

Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set

Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT III

Technical Details of ARM Cortex M Processors

General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT IV

Instruction SET of ARM Cortex M

Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT V

Floating Point Operations

About Floating Point Data, Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU->FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

TEXTBOOKS

1. ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004.
2. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu, Elsevier Publications, 3rd Ed.,

REFERENCES

1. Arm System on Chip Architectures – Steve Furber, Edison Wesley, 2000.
2. ARM Architecture Reference Manual – David Seal, Edison Wesley, 2000.

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN (PE-1)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

UNIT I

MOS Design: Pseudo NMOS logic- Inverter, Inverter threshold voltage, output high voltage, Output low voltage, gain at gate threshold voltage, transient response, rise time, fall time, pseudo NMOS logic gates, transistor equivalency, CMOS inverter logic.

UNIT II

Combinational MOS logic circuits

MOS logic circuits with NMOS loads, Primitive CMOS logic gates- NOR and NAND gates, Complex logic circuits design- realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full-adder, cmos transmission gates, designing with transmission gates.

UNIT III

Sequential MOS logic circuits

Behavior of bistable elements, SR Latch, Clocked Latch and Flip-flop circuits, CMOS D Latch and edge triggered flip-flop.

UNIT IV

Dynamic Logic Circuits

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, high performance dynamic CMOS circuits.

UNIT V

Semiconductor Memories

Types, RAM array Organization, DRAM- types, operation, leakage currents in DRAM cell and refresh operation, SRAM - operation , leakage currents in SRAM cells, Flash memory- NOR flash and NAND flash.

TEXTBOOKS

1. Digital Integrated Circuit Design- Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuit Analysis and Design – Sung Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCES

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming Bo Lin, CRC Press, 2011
2. Digital Integrated Circuits: A Designs Perspective - Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

HIGH PERFORMANCE NETWORKS (PE-2)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: Computer Networks

Course Objectives

At the end of the course, the students will be able to:

1. understand of switching and data transmission.
2. Familiarize the students with the error correction and detection techniques.
3. Understanding of basic principles of Multiple Access, Frame Relay and ATM
4. Obtain the knowledge of Logical Addressing, Transport layer protocols, congestion control mechanism and Domain Name System
5. Gain an expertise in areas like Logical Network Design and routing protocols.

Course Outcomes

After completing this course the student must demonstrate the knowledge and ability to

1. Independently understand the basic data transmission and data link layer concepts.
2. Understand and explain error correction and detection.
3. Analyze the details of network layer protocols and transport layer protocols
4. Design different types of network topologies.
5. Analyze and compare various routing protocols.

UNIT I

WPANs

Bluetooth- Architecture, Bluetooth Layers, ZigBee Technology, IEEE 802.15.4 LR – WPAN Device Architecture, IEEE 802.15.3a-Ultra Wideband

WLANs

Equipment, Topologies, Technologies, IEEE 802.11 WLAN

Wireless WANs

Cellular Telephony- Frequency Reuse Principle, Transmitting, Receiving, Roaming, First Generation, Second Generation, Third Generation

UNIT II

Congestion Control and Quality of Service

Data Traffic, Congestion, Congestion Control, Quality of Service, Techniques to Improve QoS, Integrated Services, Differentiated Services, QoS in Switched Networks

Queue Management

Passive-Drop trial, Drop front, Random drop, Active- early Random drop, Random Early detection.

AD HOC WIRELESS NETWORKS

Introduction, Issues in Ad Hoc Wireless Networks

UNIT III

Quality of Service in Ad Hoc Wireless Network

Real-Time Traffic Support in Ad Hoc Wireless Networks, QoS Parameters in Ad Hoc Wireless Networks, Issues and Challenges In Providing QoS in Ad Hoc Wireless Networks - Classifications of QoS solutions- Classifications of QoS Approaches, Layer-Wise Classification of Existing QoS Solutions, Mac Layer Solutions- Cluster TDMA, IEEE802.11e, IEEE802.11 MAC Protocol-

Distributed Coordination Function, Point Coordination Function, QoS Support Mechanisms of IEEE802.11e, Enhanced Distributed Coordination Function, Hybrid Coordination Function, NETWORK LAYER SOLUTIONS-QoS Routing Protocols, Ticket-Based QoS Routing Protocol, Predictive Location-Based QoS Routing Protocol, Trigger-Based Distributed QoS Routing Protocol, QoS-Enabled Ad Hoc On-Demand Distance Vector Routing Protocol, Bandwidth Routing Protocol, On-Demand QoS Routing Protocol, On-Demand Link-State Multipath QoS Routing Protocol, Asynchronous Slot Allocation Strategies, QoS frame work for Ad Hoc Wireless Networks.

UNIT IV

QoS Models

Flexible QoS Model for Mobile Ad Hoc Networks Advantages and Disadvantages

QoS Resource Reservation Signaling MRSVP

A Resource Reservation Protocol for Cellular Networks, Limitations of Adapting MRSVP for Ad Hoc Wireless Networks,

INSIGNIA-Operation of INSIGNIA Framework, Releasing Resources in INSIGNIA, Route Maintenance, Advantages and Disadvantages, INORA- Coarse Feedback Scheme, Class-Based Fine Feedback Scheme, Advantages and Disadvantages.

SWAN

SWAN Model, Local Rate Control of Best-Effort Traffic, Source-Based Admission Control of Real-Time Traffic, Impact of Mobility and False Admission, Regulation Algorithms- Source-Based Regulation, Network-Based Regulation, Advantages and Disadvantages of SWAN, Proactive RTMAC- Operation of PRTMAC, Crossover-Time Prediction, Handling Clashes, Differentiated Services Provisioning in PRTMAC, Advantages and Disadvantages of Proactive RTMAC.

UNIT V

Wireless Sensor Networks

Introduction, Application of Sensor Network , Comparison with Ad hoc Wireless Networks, Issues and challenges in Designing a Sensor Network, Sensor Network Architecture, Layer Architecture, Cluster Architecture, Data Dissemination Flooding, Gossiping, Rumor Routing, Sequential Assignment Routing, Direct Diffusion, Sensor Protocols for Information via Negotiation, Cost- Field Approach, Geography Hash Table, Small Minimum Energy Communication Network, Data Gathering, Direct Transmission, Power Efficient Gathering for Sensor Information Systems, Binary Scheme, Chain Based Three-Level Scheme.

TEXTBOOKS

1. Ad Hoc Wireless Networks Architectures and Protocols C. Siva Ram Murthy B.S. Manoj, Prentice Hall, 6th Edition, 2008.
2. Data Communications and Networking - B. A.Forouzan, 5th edition, TMH, 2013.

REFERENCES

1. Ad Hoc and Sensor Networks Theory and Applications- Carols de Morais Cordeiro and Dharma prakash Agrawal, World Scientific
2. Wireless and Mobile Networks Concepts and Protocols- Dr. Sunil Kumar S. Manvi and Mahabaleshwar S. Kakkasageri.
3. Computer Networks, *Andrew S. Tanenbaum*, Fourth Edition, Prentice Hall.
4. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.

**MOBILE COMPUTING
(PE-2)**

M.Tech. I Year I-Semester

**L T P C
3 0 0 3**

Prerequisites: Computer Networks, Advanced Operating Systems

Course Objectives

1. To make the student understand the concept of mobile computing paradigm, its novel applications and limitations.
2. To understand the typical mobile networking infrastructure through a popular GSM protocol
3. To understand the issues and solutions of various layers of mobile networks, namely MAC layer, Network Layer & Transport Layer
4. To understand the database issues in mobile environments & data delivery models.
5. To understand the ad hoc networks and related concepts.
6. To understand the platforms and protocols used in mobile environment.

Course Outcomes

1. Able to think and develop new mobile application.
2. Able to take any new technical issue related to this new paradigm and come up with a solution(s).
3. Able to develop new ad hoc network applications and/or algorithms/protocols.
4. Able to understand & develop any existing or new protocol related to mobile environment

UNIT I

Introduction

Mobile Communications, Mobile Computing – Paradigm, Promises/Novel Applications and Impediments and Architecture; Mobile and Handheld Devices, Limitations of Mobile and Handheld Devices. GSM – Services, System Architecture, Radio Interfaces, Protocols, Localization, Calling, Handover, Security, New Data Services, GPRS, CSHSD, DECT.

UNIT II

(Wireless) Medium Access Control (MAC)

Motivation for a specialized MAC (Hidden and exposed terminals, Near and far terminals), SDMA, FDMA, TDMA, CDMA, Wireless LAN/(IEEE 802.11)

Mobile Network Layer

IP and Mobile IP Network Layers, Packet Delivery and Handover Management, Location Management, Registration, Tunneling and Encapsulation, Route Optimization, DHCP.

UNIT III

Mobile Transport Layer

Conventional TCP/IP Protocols, Indirect TCP, Snooping TCP, Mobile TCP, Other Transport Layer Protocols for Mobile Networks.

Database Issues

Database Hoarding & Caching Techniques, Client-Server Computing & Adaptation, Transactional Models, Query processing, Data Recovery Process & QoS Issues.

UNIT IV

Data Dissemination and Synchronization

Communications Asymmetry, Classification of Data Delivery Mechanisms, Data Dissemination, Broadcast Models, Selective Tuning and Indexing Methods, Data Synchronization – Introduction, Software, and Protocols

UNIT V

Mobile Ad hoc Networks (MANETs)

Introduction, Applications & Challenges of a MANET, Routing, Classification of Routing Algorithms, Algorithms such as DSR, AODV, DSDV, Mobile Agents, Service Discovery.

Protocols and Platforms for Mobile Computing

WAP, Bluetooth, XML, J2ME, JavaCard, PalmOS, Windows CE, Symbian OS, Linux for Mobile Devices, Android.

TEXTBOOKS

1. Jochen Schiller, “Mobile Communications”, Addison-Wesley, Second Edition, 2009.
2. Raj Kamal, “Mobile Computing”, Oxford University Press, 2007, ISBN: 0195686772

REFERENCES

1. The CDMA 2000 System for Mobile Communications – Vieri Vaughi, Alexander Damn Jaonvic – Pearson.
2. Adalestein - Fundamentals of Mobile & Parvasive Computing, 2008, TMH.

**ARTIFICIAL INTELLIGENCE
(PE-2)**

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite

Course Objectives

1. To learn the difference between optimal reasoning vs human like reasoning
2. To understand the notions of state space representation, exhaustive search, heuristic search along with the time and space complexities
3. To learn different knowledge representation techniques
4. To understand the applications of AI: namely Game Playing, Theorem Proving, Expert Systems, Machine Learning and Natural Language Processing

Course Outcomes

1. Possess the ability to formulate an efficient problem space for a problem expressed in English.
2. Possess the ability to select a search algorithm for a problem and characterize its time and space complexities.
3. Possess the skill for representing knowledge using the appropriate technique.
4. Possess the ability to apply AI techniques to solve problems of Game Playing, Expert Systems, Machine Learning and Natural Language Processing.

UNIT I

Introduction, History, Intelligent Systems, Foundations of AI, Sub areas of AI, Applications. Problem Solving – State-Space Search and Control Strategies: Introduction, General Problem Solving, Characteristics of Problem, Exhaustive Searches, Heuristic Search Techniques, Iterative-Deepening A*, Constraint Satisfaction. Game Playing, Bounded Look-ahead Strategy and use of Evaluation Functions, Alpha-Beta Pruning

UNIT II

Logic Concepts and Logic Programming

Introduction, Propositional Calculus, Propositional Logic, Natural Deduction System, Axiomatic System, Semantic Tableau System in Propositional Logic, Resolution Refutation in Propositional Logic, Predicate Logic, Logic Programming. Knowledge Representation: Introduction, Approaches to Knowledge Representation, Knowledge Representation using Semantic Network, Extended Semantic Networks for KR, Knowledge Representation using Frames.

UNIT III

Expert System and Applications

Introduction, Phases in Building Expert Systems, Expert System Architecture, Expert Systems Vs Traditional Systems, Truth Maintenance Systems, Application of Expert Systems, List of Shells and Tools. Uncertainty Measure – Probability Theory: Introduction, Probability Theory, Bayesian Belief Networks, Certainty Factor Theory, Dempster-Shafer Theory.

UNIT IV

Machine-Learning Paradigms

Introduction. Machine Learning Systems. Supervised and Unsupervised Learning. Inductive Learning. Learning Decision Trees (Text Book 2), Deductive Learning. Clustering, Support Vector Machines.

Artificial Neural Networks: Introduction, Artificial Neural Networks, Single- Layer Feed-Forward Networks, Multi-Layer Feed-Forward Networks, Radial- Basis Function Networks, Design Issues of Artificial Neural Networks, Recurrent Networks.

UNIT V

Advanced Knowledge Representation Techniques

Case Grammars, Semantic Web Natural Language Processing: Introduction, Sentence Analysis Phases, Grammars and Parsers, Types of Parsers, Semantic Analysis, Universal Networking Knowledge.

TEXTBOOKS

1. Saroj Kaushik. Artificial Intelligence. Cengage Learning, 2011.
2. Russell, Norvig: Artificial intelligence, A Modern Approach, Pearson Education, Second Edition. 2004.

REFERENCES

1. Rich, Knight, Nair: Artificial intelligence, Tata McGraw Hill, Third Edition 2009.

ADVANCED COMPUTER NETWORKS (PE-2)

M.Tech. I Year I-Semester

L T P C
3 0 0 3

Prerequisite: Computer Networks

Course Objectives

1. To study the WLAN and WPAN architecture and protocols
2. To know about WiMAX services, 802.16 standard, cellular telephony & satellite networks.
3. To study the techniques to improve QoS in Networks
4. To learn about the basic concepts of Ad hoc wireless Networks
5. To know about various Routing Protocols in Ad hoc Networks.
6. To learn the concepts of Wireless Sensor Networks, architecture and various data dissemination and data gathering techniques

Course Outcomes

At the end of the course, the student will be able to:

1. Acquire the knowledge about Wireless LANs, Bluetooth and WiMAX standards, architecture and their sub-layers.
2. Understand congestion control mechanisms and techniques to improve Quality of Service in switched networks
3. Get the basic concepts of Ad hoc wireless networks and its protocols and issues related to QoS, energy management, scalability and Security.
4. Explain about Wireless Sensor Network architecture, data dissemination & data gathering techniques and will be able to address the issues and challenges in designing Sensor Networks.

Unit I

Wireless LANs

Architectural Comparison, Characteristics, Access Control, IEEE 802.11 Project: Architecture, MAC Sub layer, Addressing Mechanism, Physical Layer

Bluetooth

Architecture, Bluetooth Layers

WiMAX

Services, IEEE Project 802.16, Cellular Telephony: operation, 1G, 2G, 3G, 4G, Satellite Networks, GEO, MEO and LEO Satellites

Unit II

Congestion Control and Quality of Service

Data Traffic, Congestion, Congestion Control, Quality of Service, Techniques to Improve QoS, Integrated Services, Differentiated Services, QoS in Switched Networks

Queue Management

Passive-Drop, Drop front, Random drop, Active-early Random drop, Random Early detection.

Unit III

AD HOC WIRELESS NETWORKS

Introduction, Cellular and Ad hoc Wireless Networks, Application of Ad Hoc Wireless Networks, Issues in Ad Hoc Wireless Networks, Medium Access Scheme, Routing, Multicasting, Transport Layer

Protocols, Pricing Scheme, Quality of Service Provisioning, Self-Organization, Security, Addressing and Service Discovery, Energy Management, Scalability, Deployment Considerations, Ad Hoc Wireless Internet

Unit IV

Quality of Service in Ad Hoc Wireless Networks

Introduction, Real Time Traffic Support in Ad Hoc Wireless Networks, QoS Parameters in Ad Hoc Wireless Network, Issues and Challenges in providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions: MAC Layer Solutions, Cluster TDMA, IEEE 802.11e, DBASE, Network Layer Solutions, QoS Routing Protocols, Ticket Based QoS Routing Protocol, Predictive Location Based QoS routing protocol, Trigger Based Distributed QoS Routing Protocol, QoS enabled AODV Routing Protocol, Bandwidth QoS Routing Protocol, On Demand QoS Routing Protocol, On Demand Link-State Multipath QoS Routing Protocol, Asynchronous Slot Allocation Strategies. QoS Frameworks for Ad Hoc Wireless Networks.

Unit V

Wireless Sensor Networks

Introduction, Application of Sensor Network , Comparison with Ad hoc Wireless Networks, Issues and challenges in Designing a Sensor Network, Sensor Network Architecture, Layer Architecture, Cluster Architecture, Data Dissemination Flooding, Gossiping, Rumor Routing, Sequential Assignment Routing, Direct Diffusion, Sensor Protocols for Information via Negotiation, Cost- Field Approach, Geography Hash Table, Small Minimum Energy Communication Network, Data Gathering, Direct Transmission, Power Efficient Gathering for Sensor Information Systems, Binary Scheme, Chain Based Three-Level Scheme.

TEXTBOOKS

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI
2. Data Communications and Networking - B. A.Forouzan, 5th , 2013, TMH.

REFERENCES

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.

EMBEDDED SYSTEMS LABORATORY

M.Tech. I Year I-Semester

L T P C

0 0 4 2

List of Experiments

- 1. Functional Testing Of Devices**
Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
- 2. Exporting Display On To Other Systems**
Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
- 3. GPIO Programming**
Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
- 4. Interfacing Chronos eZ430**
Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
- 5. ON/OFF Control Based On Light Intensity**
Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
- 6. Battery Voltage Range Indicator**
Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)
- 7. Dice Game Simulation**
Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
- 8. Displaying RSS News Feed On Display Interface**
Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
- 9. Porting Openwrt To the Device**
Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
- 10. Hosting a website on Board**
Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server(eg: Apache) and thereby host the website.
- 11. Webcam Server**
Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
- 12. FM Transmission**
Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Note : Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

SIMULATION LABORATORY

M.Tech. I Year I-Semester

L	T	P	C
0	0	4	2

I. Student has to design his/her user defined library components by using and standard HDL simulator and Synthesis tool for target FPGA device.

II. Combinational Logic Circuits

- Generic Multiplexer.
- Generic Priority Encoder.
- Design of RAM Memory.
- Code Converters.

Combinational Arithmetic circuits

- Ripple Carry Adder.
- Carry-Look ahead adder.
- Signed and Unsigned Adders.
- Signed and Unsigned Subtractors.
- N-bit Comparator.
- N – bit Arithmetic Logic Unit.
- Parallel Signed and unsigned Multipliers.
- Dividers.

III. Sequential Circuits

- Shift Register with Load.
 - Switch Debouncer.
 - Timer.
 - Fibonacci Series Generator.
 - Frequency Meters.
- Student has to design his/her user Library consisting of following circuits / components. (use any Standard HDL simulator and synthesis tool for a target FPGA device available in Lab.)

The library components required

1. Adders, Subtractors, Multiplexers, Decoders, Encoders, code converters, n-bit adders – Ripple Carry adders, carry – look ahead adder, n-bit comparator, n-bit ALU, Multipliers, MAC units.
2. Different Latches & Flip-flops, shift Registers, Converters, Sequence generators, Sequence detector, 2D-memory devices, clock generators, clock dividers, e.t.c
3. At the end each student has to design an application hardware using these components in library.

RESEARCH METHODOLOGY AND IPR

M.Tech. I Year I-Semester

L	T	P	C
2	0	0	0

Course Objectives

1. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
2. Follow research related information
3. Understanding that when IPR would take such important place in growth of individuals and nation, it is needless to emphasis the need of information about intellectual Property Right to be promoted among students in general & engineering in particular.
4. Understand that IPR protection leads to economic growth and social benefits

Course Outcomes

At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research problem formulation.
3. Understand the IPR protection provides incentive top inventors for further research work and investment in R & D.
4. Understand that IPR protection leads to creation of new and better products.

UNIT I

Meaning of research problem, sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem, approaches of investigation of solutions for research problem.

UNIT II

Data collection, analysis, interpretation, necessary instrumentations, Effective literature studies approaches, analysis Plagiarism, and Research ethics

UNIT III

Effective technical writing, how to write report, paper, Developing a research proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT IV

Nature of Intellectual property

Patents, Designs, Trade and Copyright, Process of Patenting and Development - technological research, innovation, patenting, development. International Scenario- International cooperation on intellectual property, Procedure for grants of patents, Patenting under PCT.

UNIT V

Patents Rights

Scope of Patents Rights, Licensing and transfer of technology, Patents information and databases, Geographical Indications, Administration of Patent System, New developments in IPR - IPR of Biological Systems, Computer Software etc., Traditional Knowledge Case Studies, IPR and IITs.

REFERENCES

1. Stuart Melville and Wayne Goddard, “ Research methodology: An introduction for science & engineering students”
2. Wayne Goddard and Stuart Melville, “ Research methodology: An introduction”
3. Ranjit Kumar, 2ND Edition, “ Research methodology: A Step by Step Guide for beginners”
4. Halbert, “ Resisting Intellectual Property”, Taylor & Francis Ltd, 2007.
5. Mayall, “ Industrial Design”, McGraw Hill, 1992.
6. Niebel, “ Product Design”, McgRAW Hill, 1974.
7. Asimov, “ Introduction to Design”, Prentice Hall, 1962.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “ Intellectual Property in New Technological Age”. 2016.
9. T. Ramappa, “ Intellectual Property Rights Under WTO”, S. Chand, 2008

SYSTEM ON CHIP ARCHITECTURES

M.Tech. I Year II-Semester

L T P C
3 0 0 3

Prerequisite: Embedded System Design.

Course Objectives

The objectives of this course are:

1. To introduce the architectural features of system on chip.
2. To provides information on interconnection necessities between computational block and memory block.

Course Outcomes

On completion of this course the student will be able to:

1. Introduction to SOC Architecture and design.
2. Processor design Architectures and limitations
3. To acquires the knowledge of memory architectures on SOC.
4. To understands the interconnection strategies and their customization on SOC.

UNIT I

Introduction to the System Approach

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT II

Processors

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III

Memory Design for SOC

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I , and D – Caches , Multilevel Caches, Virtual to real translation , SOC Memory System , Models of Simple Processor – memory interaction.

UNIT IV

Interconnect Customization and Configuration

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V

Application Studies / Case Studies

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXTBOOKS

1. Computer System Design System-on-Chip by Michael J. Flynn and Wayne Luk, Wiley India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Eed., 2000, Addison Wesley Professional.

REFERENCES

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers

EMBEDDED PROGRAMMING

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: C Language Programs

Course Objectives

1. To explore the difference between general purpose programming languages and Embedded Programming Language.
2. To provide case studies for programming in Embedded systems.

Course Outcomes

1. Expected to learn the basics of Embedded C with reference to 8051.
2. Understand how to handle control and data pins at hardware level.
3. Capable of introducing into objective nature of Embedded C.
4. Understand the specifications of real time embedded programming with case studies.

UNIT I

Programming Embedded Systems in C

Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family

Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT II

Reading Switches

Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT III

Adding Structure to your Code

Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT IV

Meeting Real-Time Constraints

Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT V

Case Study

Intruder Alarm System-Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXTBOOKS

1. Embedded C by **Michael J. Pont** , A Pearson Education

REFERENCES

1. PICmicro MCU C-An introduction to programming, The Microchip PIC in CCS C By Nigel Gardner

**RELIABILITY ENGINEERING
(PE-3)**

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: None

Course Objectives

1. To comprehend the concept of Reliability and Unreliability
2. Derive the expressions for probability of failure, Expected value and standard deviation of Binominal distribution, Poisson distribution, normal distribution and weibull distributions.
3. Formulating expressions for Reliability analysis of series-parallel and Non-series parallel systems
4. Deriving expressions for Time dependent and Limiting State Probabilities using Markov models.

Course Outcomes

Upon the completion of this course, the student will be able to

1. Apply fundamental knowledge of Reliability to modeling and analysis of series-parallel and Non-series parallel systems.
2. Solve some practical problems related with Generation, Transmission and Utilization of Electrical Energy.
3. Understand or become aware of various failures, causes of failures and remedies for failures in practical systems.

Unit I

Rules for combining probabilities of events, Definition of Reliability. Significance of the terms appearing in the definition. Probability distributions: Random variables, probability density and distribution functions. Mathematical expectation, Binominal distribution, Poisson distribution, normal distribution, weibull distribution.

Unit II

Hazard rate, derivation of the reliability function in terms of the hazard rate. Failures: Causes of failures, types of failures (early failures, chance failures and wear-out failures). Bath tub curve. Preventive and corrective maintenance. Modes of failure. Measures of reliability: mean time to failure and mean time between failures.

Unit III

Classification of engineering systems: series, parallel and series-parallel systems- Expressions for the reliability of the basic configurations.

Reliability evaluation of Non-series-parallel configurations: Decomposition, Path based and cutest based methods, Deduction of the Paths and cut sets from Event tree.

Unit IV

Discrete Markov Chains: General modeling concepts, stochastic transitional probability matrix, time dependent probability evaluation and limiting state probability evaluation of one component repairable model. Absorbing states.

Continuous Markov Processes: Modeling concepts, State space diagrams, Stochastic Transitional Probability Matrix, Evaluating time dependent and limiting state Probabilities of one component repairable model. Evaluation of Limiting state probabilities of two component repairable model.

UNIT V

Approximate system Reliability analysis of Series systems, parallel systems with two and more than two components, Network reduction techniques. Minimal cutest/failure mode approach.

TEXTBOOKS

1. "Reliability evaluation of Engineering systems", Roy Billinton and Ronald N Allan, BS Publications.
2. "Reliability Engineering", Elsayed A. Elsayed, Prentice Hall Publications.

REFERENCES

1. "Reliability Engineering: Theory and Practice", By Alessandro Birolini, Springer Publications.
2. "An Introduction to Reliability and Maintainability Engineering", Charles Ebeling, TMH Publications.
3. "Reliability Engineering", E. Balaguruswamy, TMH Publications.

**INTELLIGENT CONTROL
(PE-3)**

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: None

Course Objectives

1. Gaining an understanding of the functional operation of a variety of intelligent control techniques and their bio-foundations
2. The study of control-theoretic foundations
3. Learning analytical approaches to study properties

Course Outcomes

Upon the completion of this course, the student will be able to

1. Develop Neural Networks, Fuzzy Logic and Genetic algorithms.
2. Implement soft computing to solve real-world problems mainly pertaining to control system applications

Unit I

Introduction and motivation. Approaches to intelligent control. Architecture for intelligent control. Symbolic reasoning system, rule-based systems, the AI approach. Knowledge representation. Expert systems.

Unit II

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feedforward Multilayer Perceptron. Learning and Training the neural network. Data Processing: Scaling, Fourier transformation, principal-component analysis.

Unit III

Networks: Hopfield network, Self-organizing network and Recurrent network. Neural Network based controller Case studies: Identification and control of linear and nonlinear dynamic systems using Matlab-Neural Network toolbox. Stability analysis of Neural-Network interconnection systems.

Unit IV

Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters. Solution of typical control problems using genetic algorithm. Concept on some other search techniques like tabu search and ant-colony search techniques for solving optimization problems.

Unit V

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control. Fuzzification, inferencing and defuzzification. Fuzzy knowledge and rule bases. Fuzzy modeling and control schemes for nonlinear systems. Fuzzy logic control for nonlinear time-delay system. Implementation of fuzzy logic controller using Matlab fuzzy-logic toolbox. Stability analysis of fuzzy control systems.

TEXTBOOKS

1. Simon Haykins, Neural Networks: A comprehensive Foundation, Pearson Edition, 2003.
2. T.J.Ross, Fuzzy logic with Fuzzy Applications, Mc Graw Hill Inc, 1997.
3. David E Goldberg, Genetic Algorithms.
4. John Yen and Reza Langari, Fuzzy logic Intelligence, Control, and Information, Pearson Education, Indian Edition, 2003.

REFERENCES

1. M.T.Hagan, H. B. Demuth and M. Beale, Neural Network Design, Indian reprint, 2008.
2. Fredric M.Ham and Ivica Kostanic, Principles of Neurocomputing for science and Engineering, McGraw Hill, 2001.
3. N.K. Bose and P.Liang, Neural Network Fundamentals with Graphs, Algorithms and Applications, Mc - Graw Hill, Inc. 1996.
4. Yung C. Shin and Chengying Xu, Intelligent System - Modeling, Optimization and Control, CRC Press, 2009.
5. N.K.Sinha and Madan M Gupta, Soft computing & Intelligent Systems - Theory & Applications, Indian Edition, Elsevier, 2007.
6. Witold Pedrycz, Fuzzy Control and Fuzzy Systms, Overseas Press, Indian Edition, 2008

SENSORS AND ACTUATORS (PE-3)

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: None

Course Objectives

1. To Learn about Electro mechanical sensors.
2. To Learn the use of the thermal sensors and magnetic sensors for embedded system.
3. To learn the basics of radiation sensors, smart sensors and actuators.

Course Outcomes

1. Students will gain knowledge to interface various sensors and actuators in embedded applications.

UNIT I

Sensors/Transducers

Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization.

Mechanical and Electromechanical Sensors

Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors.

UNIT II

Thermal Sensors

Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors.

Magnetic sensors

Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors – Anisotropic Magnetoresistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors – Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros – Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors.

UNIT III

Radiation Sensors

Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors.

Electro analytical Sensors

Introduction – The Electrochemical Cell – The Cell Potential - Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media.

UNIT IV

Smart Sensors

Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation.

Sensors –Applications

Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring.

UNIT V

Actuators

Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators.

Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection.

Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors.

TEXTBOOKS

1. Patranabis – “Sensors and Transducers” –PHI Learning Private Limited.
2. W. Bolton – “Mechatronics” –Pearson Education Limited.

MODERN CONTROL THEORY
(PE-3)

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: Control Systems

Course Objectives

1. To explain the concepts of basics and modern control system for the real time analysis and design of control systems.
2. To explain the concepts of state variables analysis.
3. To study and analyze non linear systems.
4. To analyze the concept of stability for nonlinear systems and their categorization.
5. To apply the comprehensive knowledge of optimal theory for Control Systems.

Course Outcomes

Upon completion of this course, students should be able to:

1. Various terms of basic and modern control system for the real time analysis and design of control systems.
2. To perform state variables analysis for any real time system.
3. Apply the concept of optimal control to any system.
4. Able to examine a system for its stability, controllability and observability.
5. Implement basic principles and techniques in designing linear control systems.
6. Formulate and solve deterministic optimal control problems in terms of performance indices.
7. Apply knowledge of control theory for practical implementations in engineering and network analysis.

UNIT I

Mathematical Preliminaries and State Variable Analysis

Fields, Vectors and Vector Spaces – Linear combinations and Bases – Linear Transformations and Matrices – Scalar Product and Norms – Eigen values, Eigen Vectors and a Canonical form representation of Linear systems – The concept of state – State space model of Dynamic systems – Time invariance and Linearity – Non uniqueness of state model – State diagrams for Continuous-Time State models - Existence and Uniqueness of Solutions to Continuous-Time State Equations – Solutions of Linear Time Invariant Continuous-Time State Equations – State transition matrix and its properties. Complete solution of state space model due to zero input and due to zero state.

UNIT II

Controllability and Observability

General concept of controllability – Controllability tests, different state transformations such as diagonalization, Jordan canonical forms and Controllability canonical forms for Continuous-Time Invariant Systems – General concept of Observability – Observability tests for Continuous-Time Invariant Systems – Observability of different State transformation forms.

UNIT III

State Feedback Controllers and Observers

State feedback controller design through Pole Assignment, using Ackkermans formula– State observers: Full order and Reduced order observers.

UNIT IV

Non-Linear Systems

Introduction – Non Linear Systems - Types of Non-Linearities – Saturation – Dead-Zone - Backlash – Jump Phenomenon etc; Linearization of nonlinear systems, Singular Points and its types– Describing function–describing function of different types of nonlinear elements, – Stability analysis of Non-Linear systems through describing functions. Introduction to phase-plane analysis, Method of Isoclines for Constructing Trajectories, Stability analysis of nonlinear systems based on phase-plane method.

UNIT V

Stability Analysis

Stability in the sense of Lyapunov, Lyapunov's stability and Lypanov's instability theorems - Stability – Analysis of the Linear continuous time invariant systems by Lyapunov second method – Generation of Lyapunov functions – Variable gradient method – Krasooviski's method.

TEXTBOOKS

1. M.Gopal, Modern Control System Theory, New Age International - 1984
2. Ogata. K, Modern Control Engineering, Prentice Hall - 1997
3. N K Sinha, Control Systems, New Age International – 3rd edition.

REFERENCES

1. Donald E.Kirk, Optimal Control Theory an Introduction, Prentice - Hall Network series - First edition.

**DESIGN OF FAULT TOLERANT SYSTEMS
(PE-4)**

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: Digital System Design with PLDS

Course Objectives

1. To provide or broad understanding of fault diagnosis and tolerant design Approach.
2. To illustrate the framework of test pattern generation using semi and full automatic approach.

Course Outcomes

On completion of this course the student will be able to:

1. To acquire the knowledge of fundamental concepts in fault tolerant design.
2. Design requirements of self check-in circuits
3. Test pattern generation using LFSR
4. Design for testability rules and techniques for combinational circuits
5. Introducing scan architectures.
6. Design of built-in-self test.

UNIT I

Fault Tolerant Design

Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.

Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts. [TEXTBOOK-1]

UNIT II

Self Checking circuits & Fail safe Design

Self Checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design. [TEXTBOOK-1]

UNIT III

Design for Testability

Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.

Design for testability by means of scan

Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.[TEXTBOOK-2]

UNIT IV

Logic Built-in-self-test

BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback

shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralized and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results. [TEXTBOOK-2]

UNIT V

Standard IEEE Test Access Methods

Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language. [TEXTBOOK-2]

TEXTBOOKS

1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala, 1984,PHI
2. Digital System Test and Testable Design using HDL models and Architectures -Zainalabedin Navabi, Springer International Edition.

REFERENCES

1. Digital Systems Testing and Testable Design-Miron Abramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books
2. Essentials of Electronic Testing- Bushnell & Vishwani D.Agarwal,Springers.
3. Design for Test for Digital IC's and Embedded Core Systems- Alfred L. Crouch, 2008, Pearson Education.

EMBEDDED SOFTWARE ENGINEERING
(PE – 4)

M.Tech. I Year II-Sem

L T P C
3 0 0 3

UNIT I

Software Engineering of Embedded and Real-Time Systems

Software engineering, Embedded systems, Embedded systems are reactive systems, Real-time systems, Soft and Hard Real-Time systems, Efficient execution and the execution environment, Resource management, Challenges in real-time system design.

UNIT II

The embedded system software build process, Distributed and multi-processor architectures, Software for embedded systems, Super loop architecture, Power-save super loop, Window lift embedded design, Hardware abstraction layers (HAL) for embedded systems, HW/SW prototyping, Industry design chain, Different types of virtual prototypes, Architecture virtual prototypes, Software virtual prototypes.

UNIT III

Events, Triggers and Hardware Interface to Embedded Software

Events and triggers, Event system, Event handle, Event methods, Event data structure, Reentrancy, Disable and enable interrupts, Semaphores, Implementation with Enter/ExitCritical, Event processing, Integration, Triggers, Blinking LED, Design idea, Tick timer, Trigger interface, Trigger descriptor, Data allocation, SetTrigger, IncTicks, Making it reentrant, Initialization, Real-time aspects, Introduction to Hardware Interface, Collaboration, System integration, Launching tasks in hardware, Debug hooks, Compile-time switches, Build-time switches, Run-time switches, Self-adapting switches, Difficult hardware interactions, Testing and troubleshooting.

UNIT IV

Embedded Software Programming and Operating Systems

Introduction, Principles of high-quality programming, Readability, Maintainability, Testability, Starting the embedded software project, Libraries from third parties, Team programming guidelines, Syntax standard, Conditional compilation, Foreground/background systems, Real-time kernels, RTOS (real-time operating system), Critical sections, Task management, Preemptive scheduling, Context switching, Interrupt management, Non-kernel-aware interrupt service routine (ISR), Processors with multiple interrupt priorities, The clock tick (or system tick), Wait lists, Time management, Resource management, Synchronization, Message passing, Flow control, Clients and servers, Memory management

UNIT V

Software Reuse and Performance Engineering in Embedded Systems

Kinds of software reuse, Implementing reuse by layers, Arbitrary extensibility, Ebedded Software for Performance, The code optimization process, Using the development tools, Compiler optimization

TEXTBOOKS

1. Software Engineering for Embedded Systems: Methods, Practical Techniques, and Applications, by Oshana, Robert; Kraeling, Mark, “Newnes” Publishers, 2013.

**EMBEDDED REAL TIME OPERATING SYSTEMS
(PE-4)**

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: Computer Organization and Operating System

Course Objectives

The objectives of this course are:

1. To provide broad understanding of the requirements of Real Time Operating Systems.
2. To make the student understand, applications of these Real Time features using case studies.

Course Outcomes

1. Be able to explain real-time concepts such as preemptive multitasking, task priorities, priority inversions, mutual exclusion, context switching, and synchronization, interrupt latency and response time, and semaphores.
2. Able describe how a real-time operating system kernel is implemented.
3. Able explain how tasks are managed.
4. Explain how the real-time operating system implements time management.
5. Discuss how tasks can communicate using semaphores, mailboxes, and queues.
6. Be able to implement a real-time system on an embedded processor.
7. Be able to work with real time operating systems like RT Linux, Vx Works, MicroC /OS- II, Tiny Os

UNIT – I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT – II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.

Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT – III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT – IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT – V

Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOKS

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCES

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

HARDWARE AND SOFTWARE CO-DESIGN (PE-4)

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: Advanced Computer Architecture, Embedded System Design.

Course Objective:

1. To provide a broad understanding of the specific requirement of Hardware and software integration for embedded system

Course Outcomes:

1. To acquire the knowledge on various models
2. To explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools
4. Understand validation methods and adaptability.

UNIT –I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT –II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCES

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

EMBEDDED PROGRAMMING LABORATORY

M.Tech. I Year II-Semester

L	T	P	C
0	0	4	2

List of Programs:

1. Write a simple program to print “hello world”
2. Write a simple program to show a delay.
3. Write a loop application to copy values from P1 to P2
4. Write a c program for counting the no of times that a switch is pressed & released.
5. Illustrate the use of port header file (port M) using an interface consisting of a keypad and liquid crystal display.
6. Write a program to create a portable hardware delay.
7. Write a c program to test loop time outs.
8. Write a c program to test hardware based timeout loops.
9. Develop a simple EOS showing traffic light sequencing.
10. Write a program to display elapsed time over RS-232 link.
11. Write a program to drive SEOS using Timer 0.
12. Develop software for milk pasteurization system.

Mini Project

Develop & implement a program for intruder alarm system.

SCRIPTING LANGUAGES LABORATORY

M.Tech. I Year II-Semester

L	T	P	C
0	0	4	2

Prerequisites: Students should install Python on Linux platform.

List of Programs

Part: I

Preliminary Exercises:

1. To demonstrate different number data types in Python.
2. To perform different Arithmetic Operations on numbers in Python.
3. To create, concatenate and print a string and accessing sub-string from a given string.
4. Write a python script to print the current date in the following format “Sun May 29 02:26:23 IST 2017”
5. To demonstrate working with dictionaries in python.
6. To find largest of three numbers.
7. Write a Python program to construct the a pattern, using a nested for loop.
8. Write a Python script that prints prime numbers less than 20.
9. To convert temperatures to and from Celsius, Fahrenheit.

Part: II

10. To create, append, and remove lists in python.
11. To demonstrate working with tuples in python.
12. To find factorial of a number using Recursion.
13. Write a Python class to implement pow(x, n)
14. Write a script named copyfile.py. This script should prompt the user for the names of two text files. The contents of the first file should be input and written to the second file.
15. Write a program that inputs a text file. The program should print all of the unique words in the file in alphabetical order.
16. Write a Python class to find the frequency of each alphabet (of any language) in the given text document.

EMBEDDED NETWORKS **(PE-5)**

M.Tech. I Year III-Semester

L	T	P	C
3	0	0	3

Prerequisite: Computer Networks.

Course Objectives:

1. To elaborate on the conceptual frame work of physical layer and topological issues of networking in Embedded Systems.
2. To emphasis on issues related to guided and unguided media with specific reference to Embedded device level connectivity.

Course Outcomes :

1. Expected to acquire knowledge on communication protocols of connecting Embedded Systems.
2. Expected to master the design level parameters of USB and CAN bus protocols.
3. Understand the design issues of Ethernet in Embedded networks.
4. Acquire the knowledge of wireless protocols in Embedded domain.

UNIT –I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT –II

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXTBOOKS

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PC's parallel printer port - Jan Axelson, Penram Publications, 1996.

REFERENCES

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series -Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari□, Cambridge press 2005.

COMMUNICATION BUSES AND INTERFACES (PE-5)

M.Tech. I Year III-Semester

**L T P C
3 0 0 3**

UNIT I

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features

Limitations and applications of RS232, RS485, I²C , SPI

UNIT II

CAN

ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

UNIT III

PCIe

Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT IV

USB

Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

UNIT V

Data streaming Serial Communication Protocol- Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

TEXTBOOKS

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Ports and Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.,

REFERENCES

1. USB Complete – Jan Axelson, Penram Publications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

ROBOTICS (PE-5)

**M.Tech. I Year III-Semester
18PEC**

L	T	P	C
3	0	0	3

Prerequisite:

Introduction to Signals, Systems & Circuits
Analytical Foundations of Electronics and Communication Engineering,
Linear Systems
Elements of Control

Course Objectives

1. This introductory course is valuable for students who wish to learn about robotics through a study of industrial robot systems analysis and design.
2. This course is suited to students from engineering and science backgrounds that wish to broaden their knowledge through working on a subject that integrates multi-disciplinary technologies.

Course Outcomes

Upon the completion of this course, the student will be able to:

1. Describe the various elements that make an industrial robot system
2. Discuss various applications of industrial robot systems
3. Analyze robot manipulators in terms of their kinematics, kinetics, and control
4. Model robot manipulators and analyze their performance, through running simulations using a MATLAB-based Robot Toolbox
5. Select an appropriate robotic system for a given application and discuss the limitations of such a system
6. Program and control an industrial robot system that performs a specific task.

UNIT – I

Introduction & Basic Definitions: History of robots-robot anatomy, Coordinate Systems, Human arm Characteristics, Cartesian, Cylindrical, Polar, coordinate frames, mapping transform.

UNIT – II

Kinematics – Inverse Kinematics: Kinematics, Mechanical structure and notations, description of links and joints, Denavit-Hatzenberg notation, manipulator transformation matrix, examples inverse kinematics.

UNIT – III

Differential Motion – Statics – Dynamic Modeling: Velocity Propagation along links, manipulator Jacobian – Jacobian singularities – Lagrange Euler formulation Newton Euler formulation basics of trajectory planning.

UNIT – IV

Robot Systems : Actuators Sensors and Vision: Hydraulic and Electrical Systems Including Pumps, valves, solenoids, cylinders, stepper motors, Encoders and AC Motors Range and use of sensors, Microswitches, Resistance Transducers, Piezo-electric, Infrared and Lasers Applications of Sensors : Reed Switches, Ultrasonic, Barcode Readers and RFID – Fundamentals of Robotic vision.

UNIT – V

Robots and Applications.: Industrial Applications – Processing applications – Assembly applications, Inspection applications , Non Industrial applications.

TEXTBOOKS

1. Robotics and Control : R.K. Mittal and I.J. Nagarath, TMH 2003.
2. Introduction to Robotics – P.J. Mckerrow, ISBN: 0201182408
3. Introduction to Robotics – S. Nikv, 2001, Prentice Hall,
4. Mechatronics and Robotics: Design & Applications – A. Mutanbara, 1999, CRC Press.

REFERENCES

1. Robotics – K.S. Fu, R.C. Gonzalez and C.S.G. Lee, 2008, TMH.

**SOFT COMPUTING TECHNIQUES
(PE-5)**

M.Tech. I Year III-Sem

L	T	P	C
3	0	0	3

UNIT – I

Fundamentals of Neural Networks & Feed Forward Networks: Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT – II

Associative Memories & ART Neural Networks: Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT – III

Fuzzy Logic & Systems: Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT – IV

Genetic Algorithms: Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

UNIT – V

Hybrid Systems: Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

TEXTBOOKS

1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2. Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications -S.Rajasekaran, G.A. Vijayalakshmi Pai, July 2011, PHI, New Delhi.
3. Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.
4. Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.

REFERENCES

1. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
2. An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998
3. Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.

PRINCIPLES OF SIGNAL PROCESSING (OE)

M.Tech. I Year III-Sem

L T P C
3 0 0 3

Course Objectives

1. This gives the basics of Signals and Systems required for all Engineering related courses.
2. To understand the basic characteristics of LTI systems.
3. To know the signal transmission requirements.
4. This gives basic understanding of signal statistical properties and noise source concepts.

Course Outcomes

Upon completing this course, the student will be able to

1. Differentiate various signal functions.
2. Understand the characteristics of linear time invariant systems.
3. Understand the concepts sampling theorem.
4. Determine the Spectral and temporal characteristics of Signals.
5. Understand the concepts of Noise in Communication systems.

UNIT I

Signal Analysis

Analogy between Vectors and Signals, Orthogonal Signal Space, Signal approximation using Orthogonal functions, Mean Square Error, Closed or complete set of Orthogonal functions, Orthogonality in Complex functions, Classification of Signals and systems, Exponential and Sinusoidal signals, Concepts of Impulse function, Unit Step function, Signum function.

UNIT II

Signal Transmission through Linear Systems

Linear System, Impulse response, Response of a Linear System, Linear Time Invariant(LTI) System, Linear Time Variant (LTV) System, Transfer function of a LTI System, Filter characteristic of Linear System, Distortion less transmission through a system, Signal bandwidth, System Bandwidth, Ideal LPF, HPF, and BPF characteristics, Convolution and Correlation of Signals, Concept of convolution in Time domain and Frequency domain, Graphical representation of Convolution.

UNIT III

Sampling Theorem

Graphical and analytical proof for Band Limited Signals, Impulse Sampling, Natural and Flat top Sampling, Reconstruction of signal from its samples, Effect of under sampling – Aliasing, Introduction to Band Pass Sampling.

UNIT IV

Temporal characteristics of signals

Concept of Stationarity and Statistical Independence. First-Order Stationary Processes, Time Averages and Ergodicity, Cross Correlation and Auto Correlation of Functions, Properties of Correlation

Functions, Cross-Correlation Function and Its Properties. Power Spectrum and its Properties, Relationship between Power Spectrum and Autocorrelation Function.

UNIT V

Noise sources

Resistive/Thermal Noise Source, Arbitrary Noise Sources, Effective Noise Temperature, Noise equivalent bandwidth, Average Noise Figures, Average Noise Figure of cascaded networks, Narrow Band noise, Quadrature representation of narrow band noise & its properties.

TEXT BOOKS

1. Signals, Systems & Communications - B.P. Lathi , B.S. Publications, 2013.
2. Probability, Random Variables & Random Signal Principles - Peyton Z. Peebles, TMH, 4th Edition, 2001.

REFERENCES

1. Signals and Systems - A.V. Oppenheim, A.S. Willsky and S.H. Nawabi, 2 Ed.
2. Fundamentals of Signals and Systems - Michel J. Robert, 2008, MGH International Edition.
3. Random Processes for Engineers-Bruce Hajck, Cambridge unipress,2015
4. Statistical Theory of Communication – S.P Eugene Xavier, New Age Publications, 2003.