ACADEMIC REGULATIONS
COURSE STRUCTURE AND
DETAILED SYLLABUS

ELECTRONICS & COMMUNICATION ENGINEERING

For

M. Tech. (Digital Systems & Computer Electronics)
(Two Year Full Time Programme)

JNTUH COLLEGE OF ENGINEERING HYDERABAD
(Autonomous)
Kukatpally, Hyderabad – 500 085, Telangana, India.

2015
### I – SEMESTER

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JNTUH COLLEGE OF ENGINEERING HYDERABAD
M.Tech. (Digital Systems & Computer Electronics) – Full Time w.e.f. 2015-16

Elective – I
1. Advanced Data Communications.
2. Embedded System Design.

Elective – II
1. TCP / IP and ATM Networks.
2. CMOS Analog Integrated Circuit Design
3. Coding Theory and Techniques

Elective – III
1. Wireless Communication and Networks.
3. Soft Computing Techniques

Elective – IV
1. Embedded Real Time Operating Systems.
2. Speech and Audio Signal Processing.
3. Scripting Languages.

Elective – V
1. Advanced Computer Networks
2. System on Chip Architecture
3. Low Power VLSI Design

Elective – VI
2. CMOS Mixed Signal Design.

Elective – VII
1. High Speed Networks
2. Digital Signal Processors and Controllers
3. Image and Video Processing

Elective – VIII
1. Embedded Networks.
2. Software Defined Radio
3. Hardware - Software Co-Design.
Prerequisite: Switching Theory and Logic Design

Course Objectives:
1) To provide extended knowledge of digital logic circuits in the form of state model approach.
2) To provide an overview of system design approach using programmable logic devices.
3) To provide and understand of fault models and test methods.
4) To get exposed to the various architectural features of CPLDS and FPGAS.
5) To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6) To expose software tools used for design process with the help of case studies.

Course Outcomes:
1) To understands the minimization of Finite state machine.
2) To exposes the design approaches using ROM’s, PAL’s and PLA’s.
3) To provide in depth understanding of Fault models.
4) To understands test pattern generation techniques for fault detection.
5) To design fault diagnosis in sequential circuits.
6) To provide exposure to various CPLDS and FPGAS available in market.
7) To acquire knowledge in one hot state machine design applicable to FPGA.
8) To get exposure to EDA tools.
9) To provide understanding in the design of flow using case studies.

UNIT-I:
Programmable Logic Devices:
The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs- Altera CPLDs, FPGAs-FPGA technology, architecture, vortex CLB and slice- Stratix LAB and ALM-RAM Blocks, DSP Blocks, Clock Management, I/O standards, Additional features. [TEXTBOOK-1]

UNIT-II:
Analysis and derivation of clocked sequential circuits with state graphs and tables:
A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. [TEXTBOOK-2]

UNIT-III:
Sequential circuit Design:
Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]

UNIT-IV:
Fault Modeling and Test Pattern Generation:
Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.
Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT-V:
Fault Diagnosis in sequential circuits:
Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.1]

TEXTBOOKS:
1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
3. Logic Design Theory-N.N.Biswas PHI

REFERENCES:
2. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Digital Systems & Computer Electronics)  

VLSI TECHNOLOGY AND DESIGN

L       T       P       C
4       0       0       4

Prerequisite: VLSI, ICA

Course Objectives:
1) Students from other engineering background to get familiarize with large scale integrated technology.
2) To expose fabrication methods, layout and design rules.
3) Learn methods to improve Digital VLSI system’s performance.
4) To know about VLSI Design constraints.
5) Visualize CMOS Digital Chip Design.

Course Outcomes:
1) Review of FET fundamentals for VLSI design.
2) To acquire knowledge about stick diagrams and layouts.
3) Enable to design the subsystems based on VLSI concepts.

UNIT –I: Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II: Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III: Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV: Sequential Systems:
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V: Floor Planning:
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

REFERENCE BOOKS:
ADVANCED DATA COMMUNICATIONS
(Elective – I)

Prerequisite: Digital Communications

Course Objectives:
1. To learn about basics of Data Communication networks, different protocols, standards and layering concepts.
2. To study about error detection and correction techniques.
3. Know about link layer protocol and point to point protocols.
4. To understand Medium Access Control sub layer protocols.
5. To know about Switching circuits, Multiplexing and Spectrum Spreading techniques for data transmission.
6. To study Wired LANs different Ethernet standards.

Course Outcomes:
At the end of the course, the student will be able to:
1. Understand the concepts of Data Communication networks, different protocols, standards and layering.
2. Acquire the knowledge of error detection, forward and reverse error correction techniques.
3. Analyze link layer protocol and point to point protocols.
4. Explain and compare the performance of different MAC protocols like Aloha, CSMA, CSMA/CA, TDMA, FDMA & CDMA.
5. Understand the features and the significance of Switching circuits, Multiplexing and Spectrum Spreading for data transmission.
6. Understand the characteristics of Wired LANs and also the operation and applications of Connecting Devices.
7. Understand the services and functions of Network layer protocols.

Unit I
Data Communications, Networks and Network Types, Internet History, Standards and Administration, Protocol Layering, TCP/IP protocol suite, OSI Model. Digital Data Transmission, DTE-DCE interface.

Data Link Layer
Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol.

Unit II
Error Detection and Correction: Types of Errors, Redundancy, detection versus correction, Coding Block Coding: Error Detection, Vertical redundancy checks, longitudinal redundancy checks, Error Correction, Error correction single bit, Hamming code.
Cyclic Codes: Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum
Data Link Control: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol.

Unit III
Media Access Control (MAC) Sub Layer
Random Access, Aloha, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation, Polling-
Token Passing, Channelization - Frequency Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA).

Unit IV
Switching: Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of switch
Multiplexing and Spectrum Spreading: Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing, Spread Spectrum -Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum.

Unit V
Wired LANS: Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Giga bit Ethernet
Connecting Devices: Hubs, Link Layer Switches, Routers
Networks Layer: Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic Host Configuration Protocol (DHCP), Network Address Resolution(NATF), Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches.

TEXT BOOKS:
1. Data Communications and Networking - B. A. Forouzan, 5th, 2013, TMH.

REFERENCE BOOKS:
1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data Communications and Networking - B. A. Forouzan, 2nd, 2013, TMH.
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Digital Systems & Computer Electronics)  
EMBEDDED SYSTEMS DESIGN  
(Elective – I)  
L    T    P    C  
4    0    0    4

Prerequisite: Microprocessor and Microcontrollers

Course Objectives:
1. To differentiate between a General purpose and an Embedded System.
2. To provide knowledge on the building blocks of Embedded System.
3. To understand the requirement of Embedded firmware and its role in API.

Course Outcomes:
1. Expected to differentiate the design requirements between General Purpose and Embedded Systems.
2. Expected to acquire the knowledge of firmware design principles.
3. Expected to understand the role of Real Time Operating System in Embedded Design.
4. To acquire the knowledge and experience of task level Communication in any Embedded System.

UNIT -I: Introduction to Embedded Systems:

UNIT -II: Typical Embedded System:
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III: Embedded Firmware:
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV: RTOS Based Embedded System Design:
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V: Task Communication:
Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:
1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:
1. Embedded Systems - Raj Kamal, TMH.
4. An Embedded Software Primer - David E. Simon, Pearson Education.
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Digital Systems & Computer Electronics)  
L   T   P   C  
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NETWORK SECURITY AND CRYPTOGRAPHY  
(Elective - I)

Prerequisite: None

Course Objectives:
1. Understand the basic concept of Cryptography and Network Security, their mathematical models
2. To provide deeper understanding of application to network security, threats/vulnerabilities to networks and countermeasures
3. To create an understanding of Authentication functions the manner in which Message Authentication Codes and Hash Functions works
4. To provide familiarity in Intrusion detection and Firewall Design Principles

Course Outcomes:
After completion of this course, the student shall be able to:
1. Describe computer and network security fundamental concepts and principles
2. Identify and assess different types of threats, malware, spyware, viruses, vulnerabilities
3. Encrypt and decrypt messages using block ciphers
4. Describe the inner-workings of today's remote exploitation and penetration techniques
5. Describe the inner-workings of popular encryption algorithms, digital signatures, certificates, anti-cracking techniques, and copy-right protections
6. Demonstrate the ability to select among available network security technology and protocols such as IDS, IPS, firewalls, SSL, SSH, IPSec, TLS, VPNs, etc.
7. Analyze key agreement algorithms to identify their weaknesses

Modern Techniques : Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Block Cipher Design Principles.

Conventional Encryption  
Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

UNIT - III: Public Key Cryptography  
Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.  
Number Theory  
Prime and Relatively prime numbers, Modular arithmetic, Fermat’s and Euler’s theorems, Testing for primality, Euclid’s Algorithm, the Chinese remainder theorem, Discrete logarithms.

UNIT- IV: Message Authentication and Hash Functions  
Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.  
Hash and Mac Algorithms
MD File, Message digest Algorithm, Secure Hash Algorithm.  
**Authentication Applications**  
Kerberos, Electronic Mail Security: Pretty Good Privacy, S/MIME.  

**UNIT – V: IP Security**  
Overview, Architecture, Authentication, Encapsulating Security Payload, Key Management.  
**Intruders, Viruses and Worms**: Intruders, Viruses and Related threats.  
**Fire Walls**: Fire wall Design Principles, Trusted systems.  

**TEXT BOOKS:**  

**REFERENCE BOOKS:**  
1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)  
5. Introduction to Cryptography, Buchmann, Springer.
TCP/IP AND ATM NETWORKS
(Elective - II)

Prerequisite: Computer Networks

Course Objectives:
1. To study Network Layer Protocols, Next Generation IP protocols
3. To understand techniques to improve QoS
4. To learn about the features of ATM networks.
5. To study the various Interconnection Networks

Course Outcomes:
At the end of the course, the student will be able to:
2. Understand and analyze about UDP, TCP AND SCTP protocols, flow and error control techniques.
3. Learn congestion control mechanisms and techniques to improve Quality of Service in switched networks.
4. To understand features of Virtual circuit networks like ATM networks and their applications.
5. Design and analyze various types of Interconnection Networks, understand the functioning of Folding, Benes, Lopping bit allocation algorithms and their significance.

Unit I
Network Layer Protocols: Internet Protocol (IP), ICMPv4, Mobile IP

Unit II
User Datagram Protocol: User Datagram, UDP Services, UDP Applications
Transmission Control Protocol: TCP Services, TCP Features, Segments, TCP Connection, State Transition Diagram, Windows in TCP, Flow and Error Control, TCP Congestion Control, TCP Timers,

Unit III
Congestion Control and Quality of Service: Data Traffic, Congestion, Congestion Control, Quality of Service, Techniques to Improve QoS, Integrated Services, Differentiated Services, QoS in Switched Networks
Queue Management: Passive-Drop trial, Drop front, Random drop, Active-early Random drop, Random Early detection.
Unit IV
SONET/SDH: Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks

Unit V
Interconnection Networks
Introduction, Banyan Networks, Properties, Crossbar switch, Three stage Class networks, Rearrangeble Networks, Folding algorithm, Benes Networks, Lopping algorithm, Bit allocation algorithm.

TEXT BOOKS:
2. High Performance TCP/IP Networking –Mahabub Hassan and Raj Jain ,PHI,2005

REFERENCE BOOKS:
2. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
CMOS ANALOG INTEGRATED CIRCUIT DESIGN
(Elective – II)

Prerequisite: Analog Electronics

Course Objectives:
Analog circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology.

1. To understand most important building blocks of all CMOS analog ICs
2. To study the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs.
3. To understand specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
4. To understand the design of differential amplifiers, current amplifiers and OP AMPS.

Course Outcomes:
After studying the course, each student is expected to be able to:
1. Design basic building blocks of CMOS analog ICs.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Determine the device dimensions of each MOSFETs involved.
4. Design various amplifiers like differential, current and operational amplifiers.

UNIT -I:
MOS Devices and Modeling:

UNIT -II:
Analog CMOS Sub-Circuits:
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III:
CMOS Amplifiers:
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV:
CMOS Operational Amplifiers:
UNIT -V:
Comparators:
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

REFERENCE BOOKS:
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Digital Systems & Computer Electronics)  
CODING THEORY AND TECHNIQUES  
(Elective - II)

Prerequisite: Digital Communications

Course Objectives:
1. To acquire the knowledge in measurement of information and errors.
2. To study the generation of various code methods.
3. To study the various application of codes.

Course Outcomes:
1. Learning the measurement of information and errors.
2. Obtain knowledge in designing various codes like block codes, cyclic codes, convolution codes, turbo codes and space codes.

UNIT – I:  
Coding for Reliable Digital Transmission and storage  
Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.  
Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correctingCapabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - II:  
Cyclic Codes  
Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT – III:  
Convolutional Codes  
Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT – IV:  
Turbo Codes  
LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

UNIT - V: Space-Time Codes  
Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti’s schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing : General Concept, Iterative APP Preprocessing and Per-layer
Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

TEXT BOOKS:

REFERENCE BOOKS:
2. Digital Communications-Fundamental and Application - Bernard Sklar, PE.
4. Introduction to Error Control Codes-Salvatore Gravano-oxford
JNTUH COLLEGE OF ENGINEERING HYDERABAD

M.Tech. I Year I-Sem (Digital Systems & Computer Electronics)  L  T  P  C  
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WIRELESS COMMUNICATIONS AND NETWORKS
( Elective – III)

Prerequisite: Digital Communications

Course objectives:
The course objectives are:
1. To provide the students with the fundamental treatment about many practical and theoretical concepts that forms basic of wireless communications.
2. To equip the students with various kinds of wireless networks and its operations.
3. To prepare students to understand the concept of frequency reuse, and be able to apply it in the design of mobile cellular system.
4. To prepare students to understand various modulation schemes and multiple access techniques that are used in wireless communications,
5. To provide an analytical perspective on the design and analysis of the traditional and emerging wireless networks, and to discuss the nature of, and solution methods to, the fundamental problems in wireless networking.
6. To train students to understand the architecture and operation of various wireless wide area networks such as GSM, IS-95, GPRS and SMS.
7. To train students to understand wireless LAN architectures and operation.
8. To prepare students to understand the emerging technique OFDM and its importance in the wireless communications.

Course Outcomes:
Upon completion of the course, the student will be able to:
1. Understand the principles of wireless communications.
2. Understand fundamentals of wireless networking
3. Understand cellular system design concepts.
4. Analyze various multiple access schemes used in wireless communication.
5. Understand wireless wide area networks and their performance analysis.
6. Demonstrate wireless local area networks and their specifications.
7. Familiar with some of the existing and emerging wireless standards.
8. Understand the concept of orthogonal frequency division multiplexing.

UNIT -I:
The Cellular Concept-System Design Fundamentals

UNIT –II:
Mobile Radio Propagation: Large-Scale Path Loss

UNIT –III:
Mobile Radio Propagation: Small –Scale Fading and Multipath
Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke’s model for flat fading, spectral shape due to Doppler spread in Clarke’s model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT -IV:
Equalization and Diversity

UNIT -V:
Wireless Networks
Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparison of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, HiperLan, WLL.

TEXT BOOKS:

REFERENCE BOOKS:
1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
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DIGITAL CONTROL SYSTEMS  
(Elective - III)

Prerequisite: Control Systems

Course Objectives:
- To explain basic and digital control system for the real time analysis and design of control systems.
- To apply the knowledge state variable analysis in the design of discrete systems.
- To explain the concept of stability analysis and design of discrete time systems.

Course Outcomes:
Upon the completion of this course, the student will be able to
- Apply the concepts of Digital control systems.
- Analyze and design of discrete systems in state variable analysis.
- To relate the concepts of stability analysis and design of discrete time systems.

UNIT – I: Concept & Representation of Discrete time Systems

Z-transform:
Definition of Z-transforms – mapping between s-plane and z-plane – inverse z-transform – properties of z-transforms - ROC of z-transforms – pulse transfer function – relation between G(s) and G(z) – signal flow graph method applied to digital control systems.

UNIT- II: STATE SPACE ANALYSIS:

UNIT – III: Controllability, Observability & Stability tests
Concept of controllability, stabilizability, observability and reachability - Controllability and observability tests, Transformation of discrete time systems into controllable and observable forms.


UNIT- IV: Design of discrete time Controllers and observers
Design of discrete time controller with bilinear transformation – Realization of digital PID controller-Design of deadbeat controller; Pole placement through state feedback.

UNIT-V: STATE OBSERVERS:
Design of - Full order and reduced order observers. Study of observer based control design
TEXT BOOKS:

REFERENCES:
2. M. Gopal, Digital Control and State Variable Methods, TMH.
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SOFT COMPUTING TECHNIQUES  
( Elective - III)  

Prerequisite: None.  

Course Objectives:  
This course makes the students to Understand  
1. Fundamentals of Neural Networks & Feed Forward Networks.  
2. Associative Memories & ART Neural Networks.  

Course Outcomes:  
On completion of this course the students will be able to  
1. Identify and employ suitable soft computing techniques in classification and optimization problems.  
2. Design hybrid systems to suit a given real – life problem.  

UNIT – I: Fundamentals of Neural Networks & Feed Forward Networks  
Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network : The Perceptron Model, Multilayer Feed Forward Neural Network : Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.  

UNIT – II: Associative Memories & ART Neural Networks  
Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.  

UNIT – III: Fuzzy Logic & Systems  
Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot’s Fuzzy Cruise Controller, Air Conditioner Controller.  

UNIT – IV: Genetic Algorithms  

UNIT – V: Hybrid Systems  
Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation
Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

TEXT BOOKS:
1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers

REFERENCE BOOKS:
1. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
EMBEDDED REAL TIME OPERATING SYSTEMS  
(Elective – IV)

Prerequisite: Computer Organization and Operating Systems.

Course Objectives:
1. To provide broad understanding of the requirements of Real Time Operating Systems.
2. To make the student understand, applications of these Real Time features using case studies.

Course Outcomes:
1. To acquire knowledge on Real Time features of UNIX and LINUX.
2. To understand the basic building blocks of Real Time Operating Systems in terms of scheduling, context switching and ISR.
3. Elaborative understanding on Real Time applications using Real Time Linux, ucos2, VX works, Embedded Linux, e.t.c.

UNIT – I: Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II: Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III: Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV: Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V: Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOKS:

REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh
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SPEECH AND AUDIO SIGNAL PROCESSING  
(Elective-IV)

Prerequisite: Adaptive Signal Processing

Course Objectives:
The objectives of this course are to make the student
1. Understand the anatomy and Physiology of Speech Production system and perception model and to design an electrical equivalent of Acoustic model for Speech Production.
2. To understand the articulatory and acoustic interpretation of various phonemes and their allophones.
3. To analyze the speech in time domain and extract various time domain parameters which can be used for various applications like pitch extraction, end point detection, Speech Compression, Speech Synthesis etc.,
4. To study the concept of Homomorphic system and its use in extracting the vocal tract information from speech using Cepstrum which is a bye product of Homomorphic processing of Speech.
5. To study various Speech Signal Processing applications viz: Speech Enhancement, Speech Recognition, Speaker Recognition.
6. To study various Audio coding techniques based on perceptual modeling of the human ear.

Course Outcomes:
On completion of this course student will be able to
1. Model an electrical equivalent of Speech Production system.
2. Extract the LPC coefficients that can be used to Synthesize or compress the speech.
3. Design a Homomorphic Vocoder for coding and decoding of speech.
4. Enhance the speech and can design an Isolated word recognition system using HMM.
5. Can extract the features for Automatic speaker recognition system which can used for classification.
6. Can design basic audio coding methods for coding the audio signal.

Unit – I:
Fundamentals of Digital Speech Processing:


Unit – II:
Time Domain models for Speech Processing:
Introduction – Window considerations, Short time energy, average magnitude, average zero crossing rate, Speech vs Silence discrimination using energy and zero crossing, pitch period estimation using a parallel processing approach, the short time autocorrelation function, average magnitude difference function, pitch period estimation using the autocorrelation function.
Linear Predictive Coding (LPC) Analysis:

Unit – III:
Homomorphic Speech Processing:

Speech Enhancement:

Unit – IV:
Automatic Speech Recognition:
Basic pattern recognition approaches, parametric representation of Speech, Evaluating the similarity of Speech patterns, Isolated digit Recognition System, Continuous word Recognition system. Elements of HMM, Training & Testing of Speech using HMM.

Automatic Speaker Recognition:
Recognition techniques, Features that distinguish speakers, MFCC, delta MFCC, Speaker Recognition Systems: Speaker Verification System, Speaker Identification System, Performance Metrics.

Unit – V:
Audio Coding:

TEXT BOOKS:

REFERENCE BOOKS:
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SCRIPTING LANGUAGES  
(Elective – IV)

Prerequisite: C Programming Language.

Course Objectives:  
The goal of the course is to study:  
1. The principles of scripting languages.  
2. Motivation for and applications of scripting.  
3. Difference between scripting languages and non-scripting languages.  
4. Types of scripting languages.  
5. Scripting languages such as PERL, TCL/TK, python and BASH.  
6. Creation of programs in the Linux environment.  
7. Usage of scripting languages in IC design flow.

Course Outcomes:  
Upon learning the course, the student will have the:  
1. Ability to create and run scripts using PERL/TCL/Python in IC design flow.  
2. Ability to use Linux environment and write programs for automation of scripts in VLSI tool design flow.

Unit – 1: Linux Basics  
Introduction to Linux, File System of the Linux, General usage of Linux kernel & basic commands, Linux users and group, Permissions for file, directory and users, searching a file & directory, zipping and unzipping concepts.

Unit – 2: Linux Networking  

Unit – 3: Perl Scripting.  
Introduction to Perl Scripting, working with simple values, Lists and Hashes, Loops and Decisions, Regular Expressions, Files and Data in Perl Scripting, References & Subroutines, Running and Debugging Perl, Modules, Object – Oriented Perl.

Unit – 4: Tcl / Tk Scripting  
Tcl Fundamentals, String and Pattern Matching, Tcl Data Structures, Control Flow Commands, Procedures and Scope, Evel, Working with Unix, Reflection and Debugging, Script Libraries, Tk Fundamentals, Tk by examples, The Pack Geometry Manager, Binding Commands to X Events, Buttons and Menus, Simple Tk Widgets, Entry and List box Widgets Focus, Grabs and Dialogs.

Unit – 5: Python Scripting.  
Introduction to Python, using the Python Interpreter, More Control Flow Tools, Data Structures, Modules, Input and Output, Errors and Exceptions, Classes, Brief Tour of the Standard Library.
Text Books:
1. Python Tutorial by Guido Van Rossum, Fred L. Drake Jr. editor, Release 2.6.4
2. Practical Programming in Tcl and Tk by Brent Welch, Updated for Tcl 7.4 and Tk 4.0.
3. Teach Yourself Perl in 21 days by David Till.

Reference Books:
I. Student has to design his/her user defined library components by using and standard HDL simulator and Synthesis tool for target FPGA device.

II. Combinational Logic Circuits
- Generic Multiplexer.
- Generic Priority Encoder.
- Design of RAM Memory.
- Code Converters.

Combinational Arithmetic circuits
- Ripple Carry Adder.
- Carry-Look ahead adder.
- Signed and Unsigned Adders.
- Signed and Unsigned Subtractors.
- N-bit Comparator.
- N – bit Arithmetic Logic Unit.
- Parallel Signed and unsigned Multipliers.
- Dividers.

III. Sequential Circuits
- Shift Register with Load.
- Switch Debouncer.
- Timer.
- Fibonacci Series Generator.
- Frequency Meters.

- Student has to design his/her user Library consisting of following circuits / components. ( use any Standard HDL simulator and synthesis tool for a target FPGA device available in Lab.)

The library components required:
1. Adders, Subtractors, Multiplexers, Decoders, Encoders, code converters, n-bit adders – Ripple Carry adders, carry – look ahead adder, n-bit comparator, n-bit ALU, Multipliers, MAC units.
2. Different Latches & Flip-flops, shift Registers, Converters, Sequence generators, Sequence detector, 2D-memory devices, clock generators, clock dividers, e.t.c
3. At the end each student has to design an application hardware using these components in library.
ADVANCED COMPUTER ARCHITECTURE

Prerequisite: Computer Organization and Operating Systems.

Course Objectives:
1. Explains instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
2. Explains different classifications of instruction set architectures
3. Explains the advanced concepts such as instruction level parallelism, out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction
4. Examine software support for ILP, including VLIW and similar approaches
5. Teach memory hierarchy design issues, including caching and virtual memory approaches
6. Explains multiprocessor and parallel processing architectures
7. Gives the organization and design of contemporary processor architectures
8. As the current trend in computer architecture is towards chip-multiprocessing, the architecture of shared memory multiprocessors and chip level interconnect (network-on-chip) will be covered as future scope.

Course Outcomes:
A student who has met the objectives of the course will be able to:
1. Understand advanced computer architecture aspects
2. Describe and explain instruction level parallelism with static scheduling, out-of-order execution and network-on-chip architectures
3. Understand the architecture and limitations of chip-multiprocessing
4. Explain in detail about time-predictable computer architecture
5. Understand the operation of modern CPUs including pipelining, memory systems and busses.
6. Design and emulate a single cycle or pipelined CPU by given specifications using Hardware Description Language (HDL).
7. Write reports and make presentations of computer architecture projects

UNIT- I: Fundamentals of Computer Design
Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II: Pipelines
Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design
UNIT - III: Instruction Level Parallelism the Hardware Approach
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo’s approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach
Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV: Multi Processors and Thread Level Parallelism
Multi Processors and Thread level Parallelism - Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V: Inter Connection and Networks
Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture
Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

REFERENCE BOOKS:
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DESIGN OF FAULT TOLERANT SYSTEMS

Prerequisite: Digital System Design with PLDs

Course Objectives:
1) To provide broad understanding of fault diagnosis and tolerant design Approach.
2) To illustrate the framework of test pattern generation using semi and full automatic approach.

Course Outcomes:
1) To acquire the knowledge of fundamental concepts in fault tolerant design.
2) To acquire the knowledge of design requirements of self check-in circuits
3) To acquire the knowledge of test pattern generation using LFSR
4) To acquire the knowledge of design for testability rules and techniques for combinational circuits
5) To acquire the knowledge of scan architectures.
6) To acquire the knowledge of design of built-in-self test.

UNIT-I: Fault Tolerant Design:
Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.
Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts. [TEXTBOOK-1]

UNIT-II: Self Checking circuits & Fail safe Design:
Self Checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.
Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design. [TEXTBOOK-1]

UNIT-III: Design for Testability:
Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller’s expansion technique, use of control and syndrome testable designs.
Design for testability by means of scan:
Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.[TEXTBOOK-2]

UNIT-IV: Logic Built-in-self-test:
BIST Basics-Memory-based BIST, BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA’s, One’s counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralised and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing
coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results. [TEXTBOOK-2]

UNIT-V: Standard IEEE Test Access Methods:
Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language. [TEXTBOOK-2]

TEXTBOOKS:
1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala, 1984, PHI

REFERENCES:
1. Digital Systems Testing and Testable Design-Miron Abramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books
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M.Tech. I Year II-Sem (Digital Systems & Computer Electronics)  

ADVANCED COMPUTER NETWORKS  
(Elective – V)

Prerequisite: Computer Networks

Course Objectives:
1. To study the WLAN and WPAN architecture and protocols
2. To know about WiMAX services, 802.16 standard, cellular telephony & satellite networks.
3. To study the techniques to improve QoS in Networks
4. To learn about the basic concepts of Ad hoc wireless Networks
5. To know about various Routing Protocols in Ad hoc Networks.
6. To learn the concepts of Wireless Sensor Networks, architecture and various data dissemination and data gathering techniques

Course Outcomes:
At the end of the course, the student will be able to:
1. Acquire the knowledge about Wireless LANs, Bluetooth and WiMAX standards, architecture and their sub-layers.
2. Understand congestion control mechanisms and techniques to improve Quality of Service in switched networks
3. Get the basic concepts of Ad hoc wireless networks and its protocols and issues related to QoS, energy management, scalability and Security.
4. Explain about Wireless Sensor Network architecture, data dissemination & data gathering techniques and will be able to address the issues and challenges in designing Sensor Networks.

Unit I
Wireless LANs: Architectural Comparison, Characteristics, Access Control, IEEE 802.11
Project: Architecture, MAC Sub layer, Addressing Mechanism, Physical Layer
Bluetooth: Architecture, Bluetooth Layers

Unit II
Congestion Control and Quality of Service: Data Traffic, Congestion, Congestion Control, Quality of Service, Techniques to Improve QoS, Integrated Services, Differentiated Services, QoS in Switched Networks
Queue Management: Passive-Drop trial, Drop front, Random drop, Active- early Random drop, Random Early detection.

Unit III
Unit IV
**Quality of Service in Ad Hoc Wireless Networks:**

Unit V
**Wireless Sensor Networks**

**TEXT BOOKS:**
2. Data Communications and Networking - B. A.Forouzan, 5th , 2013, TMH.

**REFERENCE BOOKS:**
1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
Prerequisite: Embedded System Design

Course Objectives:
1) To introduce the architectural features of system on chip.
2) To imbibe the knowledge of customization using case studies.

Course Outcomes:
1) Expected to understand SOC Architectural features.
2) To acquire the knowledge on processor selection criteria and limitations
3) To acquires the knowledge of memory architectures on SOC.
4) To understands the interconnection strategies and their customization on SOC.

UNIT – I:
Introduction to the System Approach

UNIT – II:
Processors

UNIT – III:
Memory Design for SOC:

UNIT - IV:
Interconnect Customization and Configuration

UNIT – V:
Application Studies / Case Studies
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.
TEXT BOOKS:

REFERENCE BOOKS:
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM
LOW POWER VLSI DESIGN
(Selective – V)

Prerequisite: VLSI

Course Objectives:
The objectives of this course are to:
1. Identify sources of power in an IC.
2. Identify the power reduction techniques based on technology independent and technology dependent Power dissipation mechanism in various MOS logic style.
3. Identify suitable techniques to reduce the power dissipation.
4. Design adders, Multipliers and memory circuits with low power dissipation.

Course Outcomes:
1. The student will get to know the basics and advanced techniques in low power design which is a hot topic in today’s market where the power plays major role.
2. The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

UNIT –I: Fundamentals:

UNIT –II: Low-Power Design Approaches:
Switched Capacitance Minimization Approaches:
System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III: Low-Voltage Low-Power Adders:

UNIT –IV: Low-Voltage Low-Power Multipliers:
Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V: Low-Voltage Low-Power Memories:
TEXT BOOKS:
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:
AD-HOC AND WIRELESS SENSOR NETWORKS  
( Elective - VI )

Prerequisite: Wireless Sensor Networks

Course Objectives:
1. To study the fundamentals of wireless Ad-Hoc Networks.
2. To study the operation and performance of various Adhoc wireless network protocols.
3. To study the architecture and protocols of Wireless sensor networks.

Course Outcomes:
1. Students will be able to understand the basis of Ad-hoc wireless networks.
2. Students will be able to understand design, operation and the performance of MAC layer protocols of Adhoc wireless networks.
3. Students will be able to understand design, operation and the performance of routing protocol of Adhoc wireless network.
4. Students will be able to understand design, operation and the performance of transport layer protocol of Adhoc wireless networks.
5. Students will be able to understand sensor network Architecture and will be able to distinguish between protocols used in Adhoc wireless network and wireless sensor networks.

UNIT - I:
Wireless LANs and PANs

AD HOC WIRELESS NETWORKS
Introduction, Issues in Ad Hoc Wireless Networks.

UNIT - II:
MAC Protocols

UNIT - III: Routing Protocols

UNIT – IV: Transport Layer Protocols
UNIT – V:
Wireless Sensor Networks

TEXT BOOKS:

REFERENCE BOOKS:
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CMOS MIXED SIGNAL DESIGN
(Elective – VI)

Prerequisite: Analog Electronics

Course Objectives:
The objectives of this course are to:
1. Introduce circuit design concepts for basic building blocks used in mixed-signal integrated circuit designs.
2. Provide students with the skills to design mixed-signal integrated circuits with these building blocks.
3. Understand design and operation of basic analog circuits
4. Know mixed signal circuits like DAC, ADC, PLL etc.
5. Design and analysis of switched capacitor circuits
6. Analysis basic data conversion algorithms and circuits.

Course Outcomes:
At the completion of this course, each student will have demonstrated proficiency in:
1. Designing CMOS analog circuits to achieve performance specifications;
2. Analyzing CMOS based switched capacitor circuits;
3. Understanding basics of data converters
4. Understanding mixed-signal design flow

UNIT -I:
Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II:
Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT -III:
Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:
Nyquist Rate A/D Converters:
UNIT V:
Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

REFERENCE BOOKS:
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ALGORITHMS FOR VLSI DESIGN AUTOMATION
       (Elective-VI)

Prerequisite: VLSI

Course Objectives: The objectives of this course are to

1. To provide knowledge on broad spectrum of issues related to design automation of VLSI circuits.
2. To provide exposure to various tools and their applications in design automation.

Course Outcomes:
1. Expected to learn graph theory and its applications.
2. To understand the methods of combinational circuit optimization.
3. To learn optimization approaches in synthesis and verification.
4. To expose design automation using FPGA.
5. To study elaborately on physical design automation.

UNIT I:
PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II:
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION
Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III:
LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING
Problems, Concepts and Algorithms. MODELLING AND SIMULATION
Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT IV:
LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis
HIGH-LEVEL SYNTHESIS

UNIT V:
PHYSICAL DESIGN AUTOMATION OF FPGAs:
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs
TEXT BOOKS

REFERENCE BOOKS
JNTUH COLLEGE OF ENGINEERING HYDERABAD

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HIGH SPEED NETWORKS  (Elective - VII)

Prerequisite: Computer Networks

Course Objectives:
At the end of the course, the students will be able to:
1. understand of switching and data transmission.
2. Familiarize the students with the error correction and detection techniques.
3. Understanding of basic principles of Multiple Access, Frame Relay and ATM
4. Obtain the knowledge of Logical Addressing, Transport layer protocols, congestion control mechanism and Domain Name System
5. Gain an expertise in areas like Logical Network Design and routing protocols.

Course Outcomes:
After completing this course the student must demonstrate the knowledge and ability to
1. Independently understand the basic data transmission and data link layer concepts.
2. Understand and explain error correction and detection.
3. Analyze the details of network layer protocols and transport layer protocols
4. Design different types of network topologies.
5. Analyze and compare various routing protocols.

UNIT I
Switching and Data Transmission
ISO-OSI reference model. TCP/IP reference model, Circuit-switched networks, Datagram networks, Virtual-circuit networks, Structure of a switch, Telephone network, Dial-up modems, Digital Subscriber line, Cable TV networks

Data Link Layer
Error Detection and Correction: Introduction, Block coding, Linear Block codes, Cyclic codes, Checksum - Data Link Control: Framing, Flow and Error control, Protocols, Noiseless channels, Noisy channels, HDLC, Point-to-Point Protocol

UNIT II
Multiple Access: Random Access, Controlled Access, Channelization – Connecting Devices: Connecting LANs, Backbone Networks, Virtual LANs.

High Speed Networks

UNIT III
Network Layer

Transport Layer and Application Layer
UNIT IV
Domain Name System: Name space, Domain Name Space, Distribution of Name Space, DNS in the internet, Resolution, DNS messages, E-mail
Needs and Goals for Network Design
Analyzing Business Goals and Constraints: Using a Top-Down Network Design
Constraints, Analyzing Business Goals, Analyzing Business constraints – Analyzing

UNIT V
Logical Network Design
Designing Models for Addressing and Naming: Guidelines for Assigning Network Layer Addresses, Using a Hierarchical Model for Assigning Addresses, Designing a Model for Naming.
Selecting Switching and Routing Protocols

Text Books:
1. Data Communications and Networking, Behrouz A. Forouzan, Fourth Edition, Tata
   McGraw Hill
2. High Speed Networks and Internets – Performance and Quality of Service, William
   (CISCO Press)

Reference Books:
   Thomson.
4. Campus Network Design Fundamentals, Diane Teare, Catherine Paquet, Pearson
   Education (CISCO Press)
5. Computer Communications Networks, Mir, Pearson Education.
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M.Tech. I Year II-Sem (Digital Systems & Computer Electronics)

DIGITAL SIGNAL PROCESSORS AND CONTROLLERS
( Elective – VII )

Prerequisite: Digital Signal Processing, Microprocessors and Microcontrollers

Course Objectives:
1. To provide a comprehensive understanding of various programs of Digital Signal Processors.
2. To distinguish between the architectural differences of ARM and DSPs along with floating point capabilities.

Course Outcomes :
The students are
1. Expected to learn various Digital Signal Processors and their architectural features.
2. Explore the ARM development towards the functional capabilities of Digital Signal Processing.
3. Expected to work with ASM level programing using the instruction set.
4. To explore the selection criteria of DSP / ARM processors by understanding the functional level trade off issues.

UNIT-I: Introduction to Digital Signal Processing:
Introduction, A digital Signal – Processing system, the sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and Interpolation.

Architectures for Programmable DSP devices:
Basic Architectural features, DSP computational building blocks, Bus Architecture and Memory, Data addressing capabilities, Address generation UNIT, programmability and program execution, speed issues, features for external interfacing. [TEXTBOOK-1]

UNIT-II: Programmable Digital Signal Processors:
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX processors, memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, On-Chip peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX processors. [TEXTBOOK-1]

UNIT-III: Architecture of ARM Processors:
Introduction to the architecture, Programmer’s model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSР)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU). Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

Technical Details of ARM Processors:
General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility. [TEXTBOOK-2]
UNIT-IV:
Instruction SET: Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming. [TEXTBOOK-2]

UNIT-V: Floating Point Operations: About Floating Point Data, Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1.
ARM Cortex-M4 and DSP Applications:
DSP on a microcontroller, Dot Product example, writing optimised DSP code for the Cortex-M4-Biquad filter, Fast Fourier transform, FIR filter. [TEXTBOOK-2]

TEXTBOOKS:

REFERENCES:
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IMAGE AND VIDEO PROCESSING  
( Elective - VII )

Prerequisite: Digital Image Processing.

Course Objectives:
1. The student will be able to understand the quality improvement methods of Image.
2. To study the basic digital image and video filter operations.
3. Understand the fundamentals of Image Compression.
4. Understand the representation of video.
5. Understand the principles and methods of motion estimation.

Course Outcomes:
1. The students will learn image representation, filtering, compression.
2. Students will learn the basics of video processing, representation, motion estimation.

UNIT – I:
Fundamentals of Image Processing and Image Transforms
Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.
Image Segmentation
Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT – II:
Image Enhancement
Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.
Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

UNIT – III:
Image Compression
Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, , Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT - IV:
Basic Steps of Video Processing

UNIT – V:
2-D Motion Estimation
Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion
Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

**TEXT BOOKS:**

**REFERENCE BOOKS:**
Prerequisite: Computer Networks

Course Objectives:
1. To through the light on the requirements of Embedded Networks.
2. Understanding the role of various protocols in wired and wireless Embedded Networks.

Course Outcomes:
1. To make the students understand various Embedded Network protocols.
2. Acquires the knowledge of CAN bus design requirements.
3. To make the student aware of Ethernet design principles while building an Embedded Network.
4. To acquire the knowledge on the conceptual framework of Wireless Sensor Networks and their design requirements.

UNIT –I: Embedded Communication Protocols:

UNIT –II: USB and CAN Bus:

UNIT –III: Ethernet Basics:

UNIT –IV: Embedded Ethernet:

UNIT –V: Wireless Embedded Networking:
TEXT BOOKS:

REFERENCE BOOKS:
1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
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M.Tech. I Year II-Sem (Digital Systems & Computer Electronics)  

SOFTWARE DEFINED RADIO  
(Elective-VIII)

Prerequisite: Digital Signal Processing, TCP/IP

Course Objectives:  
The objectives of this course is  
1. To provide fundamentals and state of the art concepts in software defined radio.

Course Outcomes:  
On completion of this course, the students:  
1. Understand the design principles of software defined radio.  
2. Understand the analog RF components as front end block in implementation of SDR.  
3. Understand digital hardware architectures and development methods.  
4. Understand the radio recourse management in heterogeneous networks.  
5. Understand the object oriented representation of radio and network resources.

UNIT -I:  

UNIT -II:  
Profile and Radio Resource Management: Communication Profiles- Introduction, Communication Profiles, Terminal Profile, Service Profile, Network Profile, User Profile, Communication Profile Architecture, Profile Data Structure, XML Structure, Distribution of Profile Data, Access to Profile Data, Management of Communication Profiles, Communication Classmarks, Dynamic Classmarks for Reconfigurable Terminals, Compression and Coding, Meta Profile Data.

UNIT -III:  

UNIT -IV:  
Reconfiguration of the Network Elements: Introduction, Reconfiguration of Base Stations and Mobile Terminals, Abstract Modelling of Reconfigurable Devices, the Role of Local Intelligence in Reconfiguration, Performance Issues, Classification and Rating of Reconfigurable Hardware, Processing Elements, Connection Elements, Global Interconnect Networks, Hierarchical Interconnect Networks, Installing a New Configuration, Applying Reconfiguration Strategies, Reconfiguration Based on Comparison, Resource Recycling,
Flexible Workload Management at the Physical Layer, Optimised Reconfiguration, Optimisation Parameters and Algorithms, Optimization Algorithms, Specific Reconfiguration Requirements, Reconfiguring Base Stations, Reconfiguring Mobile Terminals

UNIT -V:  

TEXT BOOKS:

REFERENCE BOOKS:
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HARDWARE - SOFTWARE CO-DESIGN  
(Elective – VIII)

Prerequisite: Advanced Computer architecture , Embedded System Design

Course Objective:
1. To provide a broad understanding of the specific requirement of Hardware and software integration for embedded system.
2. To emphasize on the design specifications and tools in the Hardware – Software Co-design.

Course Outcomes:
1. To acquire the knowledge on various models of Co-design.
2. To explore the interrelationship between Hardware and software in an embedded system.
3. To acquire the knowledge of firmware development process and tools during Co-design.
4. Understand validation methods and adaptability.

UNIT –I:

UNIT –II:
Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures:
Architecture specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:
Compilation Techniques and Tools for Embedded Processor Architectures:
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:
Design Specification and Verification:
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:
Languages for System – Level Specification and Design-I:
System – level specification, design representation for system level synthesis, system level specification languages,
Languages for System – Level Specification and Design-II:
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.
TEXT BOOKS:

REFERENCE BOOKS:
1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer
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EMBEDDED SYSTEMS LABORATORY

List of Experiments:

1. **Functional Testing Of Devices**
   Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.

2. **Exporting Display On To Other Systems**
   Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.

3. **GPIO Programming**
   Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.

4. **Interfacing Chronos eZ430**
   Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.

5. **ON/OFF Control Based On Light Intensity**
   Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.

6. **Battery Voltage Range Indicator**
   Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)

7. **Dice Game Simulation**
   Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.

8. **Displaying RSS News Feed On Display Interface**
   Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.

9. **Porting Openwrt To the Device**
   Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.

10. **Hosting a website on Board**
    Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server(eg: Apache) and thereby host the website.

11. **Webcam Server**
    Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.

12. **FM Transmission**
    Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

**Note:** Devices mentioned in the above lists include Arduino, Raspberry Pi, Beaglebone
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SOFT SKILLS LAB
(Activity-based)

Course Objectives
➢ To improve the fluency of students in English
➢ To facilitate learning through interaction
➢ To illustrate the role of skills in real-life situations with case studies, role plays etc.
➢ To train students in group dynamics, body language and various other activities which boost their confidence levels and help in their overall personality development
➢ To encourage students develop behavioral skills and personal management skills
➢ To impart training for empowerment, thereby preparing students to become successful professionals

Learning Outcomes
➢ Developed critical acumen and creative ability besides making them industry-ready.
➢ Appropriate use of English language while clearly articulating ideas.
➢ Developing insights into Language and enrich the professional competence of the students.
➢ Enable students to meet challenges in job and career advancement.

INTRODUCTION
Definition and Introduction to Soft Skills – Hard Skills vs Soft Skills – Significance of Soft/Life/Self Skills – Self and SWOT Analysis and
1. Exercises on Productivity Development
   • Effective/ Assertive Communication Skills (Activity based)
   • Time Management (Case Study)
   • Creativity & Critical Thinking (Case Study)
   • Decision Making and Problem Solving (Case Study)
   • Stress Management (Case Study)
2. Exercises on Personality Development Skills
   • Self-esteem (Case Study)
   • Positive Thinking (Case Study)
   • Emotional Intelligence (Case Study)
   • Team building and Leadership Skills (Case Study)
   • Conflict Management (Case Study)
3. Exercises on Presentation Skills
   • Netiquette
   • Importance of Oral Presentation – Defining Purpose- Analyzing the audience-Planning Outline and Preparing the Presentation- Individual & Group Presentation- Graphical Organizers- Tools and Multi-media Visuals
   • One Minute Presentations (Warming up)
   • PPT on Project Work- Understanding the Nuances of Delivery- Body Language – Closing and Handling Questions – Rubrics for Individual Evaluation (Practice Sessions)
4. Exercises on Professional Etiquette and Communication
   • Role-Play and Simulation- Introducing oneself and others, Greetings, Apologies, Requests, Agreement & Disagreement….etc.
• Telephone Etiquette
• Active Listening
• Group Discussions (Case study)- Group Discussion as a part of Selection Procedure- Checklist of GDs
• Analysis of Selected Interviews (Objectives of Interview)
• Mock-Interviews (Practice Sessions)
• Job Application and Preparing Resume
• Process Writing (Technical Vocabulary) – Writing a Project Report- Assignments

5. Exercises on Ethics and Values
Introduction — Types of Values - Personal, Social and Cultural Values - Importance of Values in Various Contexts
• Significance of Modern and Professional Etiquette – Etiquette (Formal and Informal Situations with Examples)
• Attitude, Good Manners and Work Culture (Live Examples)
• Social Skills - Dealing with the Challenged (Live Examples)
• Professional Responsibility – Adaptability (Live Examples)
• Corporate Expectations

Note: Hand-outs are to be prepared and given to students.
Training plan will be integrated in the syllabus.
Topics mentioned in the syllabus are activity-based.

SUGGESTED SOFTWARE:
• The following software from ‘train2success.com’
  o Preparing for being Interviewed
  o Positive Thinking
  o Interviewing Skills
  o Telephone Skills
  o Time Management
  o Team Building
  o Decision making

SUGGESTED READING:
12. *The Hindu Speaks on Education* by the Hindu Newspaper