JNTUH COLLEGE OF ENGINEERING HYDERABAD
(AUTONOMOUS)
M.Tech. (Digital Systems & Computer Electronics)
ELECTRONICS AND COMMUNICATION ENGINEERING
COURSE STRUCTURE
SEMESTER - I

S. No.	Course Type	Course Title	L	T	P	Credits
1	Core 1	Digital Systems Design	3	0	0	3
2	Core 2	Embedded System Design	3	0	0	3
3	P E - 1	Professional Elective - 1	3	0	0	3
4	P E - 2	Professional Elective - 2	3	0	0	3
5	Lab 1	Digital Systems Design Lab	0	0	4	2
6	Lab 2	Embedded System Lab	0	0	4	2
7		Research Methodology and IPR	2	0	0	2
8	Aud 1	Audit Course 1:English for Research Paper Writing	2	0	0	0
		Total Credits	**16**	**0**	**8**	**18**

SEMESTER - II

S. No.	Course Type	Course Title	L	T	P	Credits
1	Core 3	FPGA Design	3	0	0	3
2	Core 4	Design of Fault Tolerant Systems	3	0	0	3
3	P E – 3	Professional Elective – 3	3	0	0	3
4	P E – 4	Professional Elective – 4	3	0	0	3
5	Lab 3	FPGA Design lab	0	0	4	2
6	Lab 4	Analog and Digital IC Design lab	0	0	4	2
7		Technical Seminar	0	0	4	2
8	Aud 2	Audit Course 2: Value Education	2	0	0	0
		Total Credits	**14**	**0**	**12**	**18**

SEMESTER - III

S. No.	Course Type	Course Title	L	T	P	Credits
1	P E – 5	Professional Elective – 5	3	0	0	3
2	O E	Open Elective	3	0	0	3
3	Dissertation	Dissertation Phase - I	0	0	20	10
		Total	**06**	**0**	**20**	**16**

SEMESTER - IV

S. No.	Course Type	Course Title	L	T	P	Credits
1	Dissertation	Dissertation Phase - II	--	--	32	16
		Total	**--**	**--**	**--**	**16**

Professional Elective -1

1. Advanced Data Communication
2. CMOS Digital Integrated Circuit Design
3. Advanced Computer Architecture
4. Embedded Real Time Operating Systems

Professional Elective -2

1. Low Power VLSI
2. CMOS Analog Integrated Circuit Design
3. Digital Signal Processors and Controllers
4. Internet Protocols and Technologies

Professional Elective -3

1. System on Chip Architectures
2. Pattern Recognition and Machine Learning
3. Mixed Signal Design
4. Advanced Operating Systems

Professional Elective -4

1. Wireless Sensor Networks
2. ANN and Deep Learning
3. Communication and Networking Technologies for IOT
4. VLSI Signal Processing

Professional Elective -5

1. Hardware and Software co-design
2. System design aspects of IOT
3. Ad-hoc and Wireless Sensor Networks
4. Algorithms for VLSI Design

Open Elective

1. Principles of Signal Processing

DIGITAL SYSTEM DESIGN

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: Switching Theory and Logic Design

Course Objectives

1 To provide extended knowledge of digital logic circuits in the form of state model approach.
2 To provide an overview of system design approach using programmable logic devices.
3 To provide and understand of fault models and test methods.
4 To get exposed to the various architectural features of CPLDS and FPGAS.
5 To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6 To expose software tools used for design process with the help of case studies.

Course Outcomes

1 To understands the minimization of Finite state machine.
2 To exposes the design approaches using ROM's, PAL's and PLA's.
3 To provide in depth understanding of Fault models.
4 To understands test pattern generation techniques for fault detection.
5 To design fault diagnosis in sequential circuits.
6 To provide exposure to various CPLDS and FPGAS available in market.
7 To acquire knowledge in one hot state machine design applicable to FPGA.
8 To get exposure to EDA tools.
9 To provide understanding in the design of flow using case studies.

UNIT I

Programmable Logic Devices

The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs- Altera CPLDs, FPGAs-FPGA technology, architecture, virtex CLB and slice- Stratix LAB and ALM-RAM Blocks, DSP Blocks, Clock Management, I/O standards, Additional features. [TEXTBOOK-1]

UNIT II

Analysis and derivation of clocked sequential circuits with state graphs and tables

A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. [TEXTBOOK-2]

UNIT III

Sequential circuit Design

Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2

UNIT IV

Fault Modeling and Test Pattern Generation

Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.

Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT V

Fault Diagnosis in sequential circuits

Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.1]

TEXTBOOKS

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth,Jr. -5th Ed.,Cengage Learning.
3. Logic Design Theory-N.N.Biswas,PHI

REFERENCES

1. Digital Circuits and Logic Design-Samuel C.LEE,PHI 2008
2. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.

EMBEDDED SYSTEMS DESIGN

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: Microprocessor and Microcontrollers

Course Objectives

1. To provide an overview of Design Principles of Embedded System.
2. To provide clear understanding about the role of firmware , operating systems in correlation with hardware systems.

Course Outcomes

1. Expected to understand the selection procedure of Processors in the Embedded domain.
2. Design Procedure for Embedded Firmware.
3. Expected to visualize the role of Real time Operating Systems in Embedded Systems
4. Expected to evaluate the Correlation between task synchronization and latency issues

UNIT I

Introduction to Embedded Systems

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT II

Typical Embedded System

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT III

Embedded Firmware

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT IV

RTOS Based Embedded System Design

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads,
Multiprocessing and Multitasking, Task Scheduling.

UNIT V

Task Communication

Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXTBOOKS

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCES

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

ADVANCED DATA COMMUNICATIONS
(PE – 1)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: Digital Communication

Course Objectives

The main objectives of the course are:

1. To learn about basics of data communication networks, different protocols, standards and layering concepts.
2. To study about error detection and correction techniques.
3. To know about link layer, point to point, medium access and control sub layer protocols.
4. To learn about characteristics of network layer protocols and functions of interconnecting devices.
5. To study about physical and electrical characteristics of Wired LAN, serial buses and to know about architecture & layers of CAN.

Course Outcomes

At the end of the course, the student will be able to:

1. Understand various transmission modes, configurations and topologies of data communication networks.
2. Analyze and compare various error detection and correction techniques of data communication networks.
3. Acquire the knowledge about the features and functions of various medium access control and network layer protocols.
4. Understand the features of WLAN, significance of communication buses, interfaces and interconnecting devices of data communication networks.

UNIT I

Data Communications, Networks and Network Types, Internet History, Standards and Administration, Protocol Layering, TCP/IP protocol suite, OSI Model, Digital Data Transmission, DTE-DCE interface.

Multiplexing

Multiplexing, Frequency Division Multiplexing, Synchronous and Statistical Time Division Multiplexing, OFDM.

Data Link Layer

Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol.

UNIT II

Error Detection and Correction

Types of Errors, Redundancy, Detection versus Correction, Coding, Block Coding-Error Detection, Vertical Redundancy Checks, Longitudinal Redundancy Checks, Error Correction- Single bit Error Correction, Hamming Code.

Cyclic Codes

Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum

Data Link Control: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol

UNIT III

Media Access Control (MAC) Sub Layer

Random Access, ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection(CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance(CSMA/CA), Controlled Access- Reservation, Polling-Token Passing, Channelization - Frequency Division Multiple Access(FDMA), Time - Division Multiple Access(TDMA),
Code - Division Multiple Access(CDMA).

UNIT IV

N**etworks Layer**

Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic Host Configuration Protocol(DHCP), Network Address Resolution(NATF), Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Router as Packet Switches.

Connecting devices

Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, Backbone Networks.

UNIT V

Wired LANS

Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Giga bit Ethernet

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features, Limitations and applications of RS232, RS485, I^2C , SPI

CAN

Architecture- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

TEXT BOOKS

1. Data Communications and Networking - B. A. Forouzan, 2nd & 5th Ed. TMH, 2013.
2. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.

REFERENCES

1. Computer Networking: A Top-Down Approach- James Kurose & Keith Ross , 7th Ed., Pearson, 2017.
2. Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.
3. Data Communications and Computer Networks- Brijendra Singh, 2nd Ed., 2008.
4. Wireless Digital Communications-Kamilo Feher, Prentice Hall,2003.

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

(PE - 1)

M.Tech. I Year I-Sem

L	T	P	C
3	0	0	3

UNIT I

MOS Design

Pseudo NMOS logic- Inverter, Inverter threshold voltage, output high voltage, Output low voltage, gain at gate threshold voltage, transient response, rise time, fall time, pseudo NMOS logic gates, transistor equivalency, CMOS inverter logic.

UNIT II

Combinational MOS logic circuits

MOS logic circuits with NMOS loads, Primitive CMOS logic gates- NOR and NAND gates, Complex logic circuits design- realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full-adder, cmos transmission gates, designing with transmission gates.

UNIT III

Sequential MOS logic circuits: Behavior of bistable elements, SR Latch, Clocked Latch and Flip-flop circuits, CMOS D Latch and edge triggered flip-flop.

UNIT IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, high performance dynamic CMOS circuits.

UNIT V

Semiconductor Memories: Types, RAM array Organization, DRAM- types, operation, leakage currents in DRAM cell and refresh operation, SRAM - operation , leakage currents in SRAM cells, Flash memory- NOR flash and NAND flash.

TEXTBOOKS

1. Digital Integrated Circuit Design- Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuit Analysis and Design – Sung Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCES

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming Bo Lin, CRC Press, 2011.
2. Digital Integrated Circuits: A Designs Perspective - Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

ADVANCED COMPUTER ARCHITECTURES
(PE -1)

M.Tech. I Year I-Sem

L	T	P	C
3	0	0	3

Pre-Requisite: Computer Organization and Operating Systems.

Course Objectives

1. Explains instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
2. Explains different classifications of instruction set architectures.
3. Explains the advanced concepts such as instruction level parallelism, , out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction.
4. Examine software support for ILP, including VLIW and similar approaches.
5. Teach memory hierarchy design issues, including caching and virtual memory approaches.
6. Explains multiprocessor and parallel processing architectures.
7. Gives the organization and design of contemporary processor architectures.
8. As the current trend in computer architecture is towards chip-multiprocessing, the architecture of shared memory multiprocessors and chip level interconnect (network-on-chip) will be covered as future scope.

Course Outcomes

A student who has met the objectives of the course will be able to

1. Understand advanced computer architecture aspects.
2. Describe and explain instruction level parallelism with static scheduling, out-of-order execution and network-on-chip architectures.
3. Understand the architecture and limitations of chip-multiprocessing.
4. Explain in detail about time-predictable computer architecture.
5. Understand the operation of modern CPUs including pipelining, memory systems and busses.
6. Design and emulate a single cycle or pipelined CPU by given specifications using Hardware Description Language (HDL).
7. Write reports and make presentations of computer architecture projects.

UNIT I

Fundamentals of Computer Design

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT II

Pipelines

Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design

Introduction, review of ABC of cache, Cache performance , Reducing cache miss penalty, Virtual memory.

UNIT III

Instruction Level Parallelism the Hardware Approach

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach

Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT IV

Multi Processors and Thread Level Parallelism

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT V

Inter Connection and Networks

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture

Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS

1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.

REFERENCES

1. John P. Shen and Miikko H. Lipasti, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs., MC Graw Hill.,
3. Advanced Computer Architecture - A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk ,Pearson Ed.,

EMBEDDED REAL TIME OPERATING SYSTEMS
(PE–1)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: Computer Organization and Operating System

Course Objectives

The objectives of this course are:

1. To provide broad understanding of the requirements of Real Time Operating Systems.
2. To make the student understand, applications of these Real Time features using case studies.

Course Outcomes

1. Be able to explain real-time concepts such as preemptive multitasking, task priorities, priority inversions, mutual exclusion, context switching, and synchronization, interrupt latency and response time, and semaphores.
2. Able explain how tasks are managed.
3. Able to explain how the real-time operating system implements time management.
4. Be able to work with real time operating systems like RT Linux, Vx Works, MicroC /OS- II, Tiny OS.

UNIT – I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT – II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.

Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT – III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT – IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT – V

Case Studies of RTOS: RT Linux, Free RTOS, Vx Works, Embedded Linux, Xenomai OS.

TEXT BOOKS

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCES

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

LOW POWER VLSI
(PE – 2)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Pre-Requisite: VLSI

Course Objectives

The objectives of this course are to:

1. Identify sources of power in an IC.
2. Identify the power reduction techniques based on technology independent and technology dependent Power dissipation mechanism in various MOS logic style.
3. Identify suitable techniques to reduce the power dissipation.
4. Design adders, Multipliers and memory circuits with low power dissipation.

Course Outcomes

Students able to

1. Understand the need of c VLSI designing.
2. Acquire a knowledge in consideration of various dissipations.
3. Design various low power adders,multipliers and memories.
4. Get knowledge in various design approaches.

UNIT I

Fundamentals

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II

Low-Power Design Approaches

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches

System Level Measures, Circuit Level Measures, Mask level Measures.

UNITIII Low-Voltage Low-Power Adders

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT IV

Low-Voltage Low-Power Multipliers

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT V

Low-Voltage Low-Power Memories

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCES

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

4.Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002

CMOS ANALOG INTEGRATED CIRCUIT DESIGN
(PE – 2)

M.Tech. I Year I-Semester

L	T	P	C
3	0	0	3

Pre-Requisite: Analog Electronics

Course Objectives

Analog circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology.

1. To understand most important building blocks of all CMOS analog Ics.
2. To study the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs.
3. To understand specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
4. To understand the design of differential amplifiers, current amplifiers and OP AMPs.

Course Outcomes

After studying the course, each student is expected to be able to

1. Design basic building blocks of CMOS analog ICs.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Determine the device dimensions of each MOSFETs involved.
4. Design various amplifiers like differential, current and operational amplifiers.

UNIT I

MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT II

Analog CMOS Sub-Circuits

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT III

CMOS Amplifiers

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT IV

CMOS Operational Amplifiers

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT V

Comparators

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCES

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

DIGITAL SIGNAL PROCESSORS AND CONTROLLERS
(PE- 2)

M.Tech. I Year I Semester

L	T	P	C
3	0	0	3

Prerequisite: Microprocessors and Micro Controllers

Course Objectives:
1. To provide a comprehensive understanding of various programs of DSP Processors.
2. To distinguish between the architectural difference of ARM and DSPs along with floatingpoint capabilities.

Course Outcomes:
The students are
1. Expected to learn various DSPs and their architectural features.
2. Explore the ARM development towards the functional capabilities of DS Processing.
3. Expected to work with ASM level program using the instruction set.
4. To explore the selection criteria of DSP / ARM processors by understanding thefunctional level trade off issues.

UNIT-I: Introduction to Digital Signal Processing:
Introduction, A digital Signal — Processing system, the sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation. Computational Accuracy in DSP Implementations- Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations
Architectures for Programmable DSP devices:
Basic Architectural features, DSP computational building blocks, Bus Architecture and Memory, Data addressing capabilities, Address generation UNIT, programmability and program execution, speed issues, features for external interfacing. [TEXTBOOK-1]

UNIT-II: Programmable Digital Signal Processors:
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX processors, memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, On-Chip peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX processors. [TEXTBOOK-1]

UNIT-III: Analog Devices Family of DSP Devices:
Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Blackfin Processor - The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals (TEXT BOOK- 3)

UNIT-IV: Architecture of ARM Processors:
Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)- Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are

exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.(TEXT BOOK - 2)

UNIT-V ARM Cortex-M Processor:

General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility. [TEXTBOOK-2]

TEXTBOOKS:

1. Digital Signal Processing- Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu, Elsevier Publications, Third edition.
3. A Practical Approach to Digital Signal Processing – K.Padmanabhan , S. Ananthi , Second Edition.

REFERENCES:

1. ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004.

INTERNET PROTOCOLS AND TECHNOLOGIES
(PE- 2)

M.Tech. I Year I Semester

L	T	P	C
3	0	0	3

Prerequisite: Computer Networks

Course Objectives

The main objectives of the course are:

1. To study the Underlying technologies, features and functions of Network Layer Protocols
2. To learn about User Datagram Protocol, Transmission Control Protocol and stream control Transmission protocol.
3. To learn about Modifications of Transport Layer Protocols for Ad Hoc Wireless Networks
4. To understand the techniques to improve QoS in Data Communication Networks

Course Outcomes

At the end of the course, the student will be able to:

1. Understand the functions of Network Layer Protocols
2. Understand the functions Transport layer protocols.
3. Acquire the knowledge about the operation and performance of modified version of TCP protocols in Ad-hoc wireless networks.
4. Learn about various mechanisms to improve QoS in data communication networks

UNIT I

Review of Underlying Technologies: Local Area Networks - Wired LANs, Wireless LANs ,Point to Point WANS, Switched WANS, X.25, Frame Relay , ATM, Connecting Devices

Network Layer Protocols

Network Layer Services**,** Packet Switching**,** Network Layer Performance, IP Datagram, Fragmentation, Options, Checksum,ICMP, Types of Messages, Message Format, Error Reporting, Query, Checksum, IGMP, Group Management, IGMP Messages, Encapsulation, IGMP Package, , ARP, ARP Package, RARP. Mobile IP, IPv6 Protocol IPv6 Addressing, , ICMPv6 Protocol, Transition from IPv4 to IPv6,

Unit-II

IPV4 Addressing: Classful Addressing- Sub netting and Super netting. Classless Addressing- Variable Length Blocks, Sub netting, Address Allocation

Delivery, Forwarding, and Routing

Delivery, Forwarding, and Routing of IP Packets, Structure of Router, Unicast Routing- Routing Algorithms: Distance Vector Routing, Link state Routing, Path- Vector routing, Unicat Routing Potocols : Internet Structure, Routing Information Protocol (RIP), Open Shortest Path First (OSPF), Border Gate way Protocol version 4 (BGP4)

UNIT III

Congestion Control and Quality of Service: Data Traffic, Congestion, Congestion Control, Quality of Service- flow characteristics, flow classes, Techniques to Improve QoS - Scheduling, Traffic Shaping, Passive Queue management Schemes – drop-tail, drop front, Random Drop Active Queue management Schemes – Early Random Drop (ERD), Random Early Detection (RED) , Resource Reservation, Admission control.

Integrated and Differentiated Services:
Integrated Services- Signaling, Flow Specification, Admission, Service Classes, Integrated Services Architecture (ISA), ISA components, ISA Services Resource Reservation (RSVP. Problems with Integrated Services, Differentiated Services-DS Field, DS configuration and Operation, Per-hop Behavior, Traffic conditioners.

UNIT IV
Transport Layer Protocols
Introduction to Transport Layer, Transport layer services, Connectionless Versus Connection Oriented Protocols, Transport Layer Protocols-Simple Protocols, Stop and Wait Protocols, Go Back N Protocol, Selective Repeat Protocol, Bidirectional Protocols-Piggybacking, Transport layer protocols: User Datagram Protocol(UDP)-User Datagram, UDP Services, UDP Applications, Transmission Control Protocol(TCP)-TCP Services, TCP Features, Segments, TCP Connection, State Transition Diagram, Windows in TCP, Flow and Error Control, TCP Timers, SCTP-SCTP Services, SCTP Features, Packet Format, An SCTP Association SCTP Flow and Error Control

UNIT V
Traditional TCP
Congestion Control, Additive Increase Multiplicative Decrease (AIMD), Slow Start, Fast recovery, fast retransmit.

TCP in Wireless Domain -Traditional TCP, TCP over wireless**,** Snoop TCP , TCP-Unaware Link Layer Indirect TCP, Mobile TCP, Explicit Loss Notification, WTCP, TCP SACK , Transaction-Oriented TCP

Transport Layer Protocols for Ad Hoc Wireless Networks
TCP Over Ad Hoc Wireless Networks-Feedback-Based TCP, TCP with Explicit Link Failure Notification, TCP-Bus, Ad Hoc TCP, Split TCP.

TEXT BOOKS

1. TCP/IP Protocol Suite-Behrouz A. Forouzan- 4th Edition, McGraw-Hill, 2010.
2. Data Communications and Networking - B. A. Forouzan, 5th edition, TMH, 2013

REFERENCES

1. Ad Hoc Wireless Networks Architectures and Protocols C. Siva Ram Murthy B.S. Manoj, Prentice Hall, 6th Edition, 2008.
2. Computer Networking: A Top-Down Approach- James Kurose & Keith Ross , 5th Ed., Pearson, 2017.
3. Mobile Communications by Jochen H. Schiller, 2nd Edition, Pearson-Wesley, 2003.

DIGITAL SYSTEM DESIGN LABORATORY

M.Tech. I Year I-Semester

L	T	P	C
0	0	4	2

I. Student has to design his/her user defined library components by using and standard HDL simulator and Synthesis tool for target FPGA device.(Logicgates,Adders/Subtractor,Flipflops)

II. Design the following logic circuits using HDL and verify the design with a test bench

1. Multiplexers: 4:1, 8:1, 16:1 in dataflow mode and structural mode.
2. Demultiplexers: 1:4, 1:8, 1:16 in dataflow mode and structural mode.
3. Priority encoder in behavioral model.
4. Decoders: 2x4, 3x8, 4x16 decoders in dataflow and structural model.
5. 2-D RAM array using for generate stateup, verify RD,RW operation.
6. Code converters – binary to BCD, BCD to gray code,BCD to excel -3 code,binary to hamming code.

III. Sequential Circuits

1. Universal 4/8-bit shift registers with load and verify the function of above registers.
2. Switch debounce circuit(with a delay).
3. 4bit timer design – generate a sequence waveform using their timer.(in behavioral model).
4. Parity bit generator.
5. Fibonacci series generator
6. Frequency devider circuit.
7. Finite state machine for sequence generator.

The library components required

1. Adders, Subtractors, Multiplexers, Decoders, Encoders, code converters, n-bit adders – Ripple Carry adders, carry – look ahead adder, n-bit comparator, n-bit ALU, Multipliers, MAC units.
2. Different Latches & Flip-flops, shift Registers, Converters, Sequence generators, Sequence detector, 2D-memory devices, clock generators, clock dividers, e.t.c

.

EMBEDDED SYSTEMS LABORATORY

M.Tech. I Year I-Semester

L	T	P	C
0	0	4	2

List of Experiments

1. **Functional Testing Of Devices**
   Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems**
   Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming**
   Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing a Bluetooth connector and control the Bluetooth operated devices(Test on atleast two devices).**
5. **ON/OFF Control Based On Light Intensity**
   Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. **Battery Voltage Range Indicator**
   Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)
7. **Dice Game Simulation**
   Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface**
   Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Openwrt To the Device**
   Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board**
    Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server(eg: Apache) and thereby host the website.
11. **Webcam Server**
    Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission**
    Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Note : Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

RESEARCH METHODOLOGY AND IPR

M.Tech. I Year I-Semester

L	T	P	C
2	0	0	2

Course Objectives:

- To understand the research problem
- To know the literature studies, plagiarism and ethics
- To get the knowledge about technical writing
- To analyze the nature of intellectual property rights and new developments
- To know the patent rights

Course Outcomes: At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT-I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.
Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II:

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT-III:

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Copyleft and Creative Commons Licensing. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-V:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCES:

1. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall , "Industrial Design", McGraw Hill, 1992.
4. Niebel , "Product Design", McGraw Hill, 1974.
5. Asimov , "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

ENGLISH FOR RESEARCH PAPER WRITING
(AUDIT COURSE-I)

M.Tech. I Year I-Semester

L	T	P	C
2	0	0	0

Course Objectives: To help students:
1. Understand the essentials of writing skills and their level of readability
2. Learn about what to write in each section
3. Ensure qualitative presentation with linguistic accuracy.

Course Outcomes: Students will be able to:
1. Understand writing skills and level of readability
2. Write title, abstract, different sections in research paper
3. Develop the skills needed while writing a research paper

Syllabus

Unit 1
Overview of a Research Paper- Planning and Preparation- Word Order- Useful Phrases - Breaking up Long Sentences-Structuring Paragraphs and Sentences -Being Concise and Removing Redundancy - Avoiding Ambiguity

Unit 2
Essential Components of a Research Paper- Abstracts- Building Hypothesis-Research Problem - Highlight Findings- Hedging and Criticizing, Paraphrasing and Plagiarism, Chapterisation

Unit 3
Introducing Review of the Literature – Methodology - Analysis of the Data-Findings - Discussion-Conclusions-Recommendations.

Unit 4
Key skills needed for writing a Title, Abstract, and Introduction

Unit 5
Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and draw Conclusions

Suggested Reading:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
Model Curriculum of Engineering & Technology PG Courses [Volume-I]
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook .
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht
Heidelberg London, 2011

****

FPGA DESIGN

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

UNIT-I

INRODUCTION TO FPGAs: Evolution of programmable devices,FPGA Design flow, Applications of FPGA.

UNIT-II

DESIGN EXAMPLES USING PLDs: Design of Universal block, Memory, Floating point Multiplier, Barrel shifter.

UNIT-III

FPGAs/CPLDs: Programming Technologies, Commercially available FPOGAs, Xilinxs Vertex and Spartan,Actel's FPGA, Alteras FPGA/CPLD.

UNIT-IV

Building blocks of FPGAs/CPLDs: Configurable Logic block functionally, Routing structures, Input/Output Block, Impact of logic block functionality on FPGA Performance, Model for measuring delay.

UNIT-V

Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row — based FPGAs, Introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures. FPGA architectural assumptions, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA.

Text Books:

1. John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.
2. Data sheets of Artix-7, Kintex-7, Virtex-7 .
3. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, Field Programmable Gate Arrays, 2nd Edition, Springer, 1992.

DESIGN OF FAULT TOLERANT SYSTEMS

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: Digital System Design with PLDS

Course Objectives

1. To provide or broad understanding of fault diagnosis and tolerant design Approach.
2. To illustrate the framework of test pattern generation using semi and full automatic approach.

Course Outcomes

On completion of this course the student will be able to:

1. To acquire the knowledge of fundamental concepts in fault tolerant design.
2. Design requirements of self check-in circuits
3. Test pattern generation using LFSR
4. Design for testability rules and techniques for combinational circuits
5. Introducing scan architectures.
6. Design of built-in-self test.

UNIT I

Fault Tolerant Design

Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.

Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts. [TEXTBOOK-1]

UNIT II

Self Checking circuits & Fail safe Design

Self Checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design. [TEXTBOOK-1]

UNIT III

Design for Testability

Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.

Design for testability by means of scan

Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.[TEXTBOOK-2]

UNIT IV

Logic Built-in-self-test

BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback

shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralized and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results. [TEXTBOOK-2]

UNIT V

Standard IEEE Test Access Methods

Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language. [TEXTBOOK-2]

TEXTBOOKS

1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala, 1984,PHI
2. Digital System Test and Testable Design using HDL models and Architectures -Zainalabedin Navabi, Springer International Edition.

REFERENCES

1. Digital Systems Testing and Testable Design-Miron Abramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books
2. Essentials of Electronic Testing- Bushnell & Vishwani D.Agarwal,Springers.
3. Design for Test for Digital IC's and Embedded Core Systems- Alfred L. Crouch, 2008, Pearson Education.

SYSTEM ON CHIP ARCHITECTURES
(PE-3)

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: Embedded System Design.

Course Objectives

The objectives of this course are:

1. To introduce the architectural features of system on chip.
2. To provides information on interconnection necessities between computational block and memory block.

Course Outcomes

On completion of this course the student will be able to:

1. Introduction to SOC Architecture and design.
2. Processor design Architectures and limitations
3. To acquires the knowledge of memory architectures on SOC.
4. To understands the interconnection strategies and their customization on SOC.

UNIT I

Introduction to the System Approach

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT II

Processors

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III

Memory Design for SOC

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I , and D – Caches , Multilevel Caches, Virtual to real translation , SOC Memory System , Models of Simple Processor – memory interaction.

UNIT IV

Interconnect Customization and Configuration

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V

Application Studies / Case Studies

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JEPG compression.

TEXTBOOKS

1. Computer System Design System-on-Chip by Michael J. Flynn and Wayne Luk, Wiely IndiaPvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Eed., 2000, Addison Wesley Professional.

REFERENCES

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, PeterPaterson and Leena Singh L, 2001, Kluwer Academic Publishers

PATTERN RECOGNITION AND MACHINE LEARNING

(PE-3)

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

UNIT-I

Introduction to Machine Learning: Human learning and its types; Machine learning and its types; well- posed learning problem; applications of machine learning; issues in machine learning.

Preparing to model: Basic data types; exploring numerical data; exploring categorical data; exploring relationship between variables; data issues and remediation; data pre-processing.

Modelling and Evaluation: Selecting a model; training model-holdout, k-fold cross-validation, bootstrap sampling; model representation and interpretability – under-fitting, over-fitting, bias-variance tradeoff; model performance evaluation – classification, regression, clustering; performance improvement.

Feature engineering: Feature construction; feature extraction; feature selection.

UNIT –II

Brief review of probability: Concept of Probability, Random Variables,Some Common Discrete Distributions:Bernoulli distributions, Binomial distribution, The multinomial and multinoulli distributions, Poission distribution, Some Common Continuous Distributions: Uniform distribution, Gaussian (normal) distribution, The laplace distribution, Multiple Random Variables: Bivariate random variables, Joint distribution Functions, Joint probability density functions, Conditional distributions, Covariance and correlation, Central Limit Theorem, Hypothesis Testing, Monte Carlo Approximation.

Bayesian Concept Learning: Bayes Theorem: Prior, Posterior, Likelihood, Bayes Theorem and Concept Learning: Brute-force Bayesian algorithm, Concept of consistent learners, Bayes optimal classifier, Naïve Bayes Classifier, Application of Naïve Bayes classifier, Handling Continuous Numeric Featurs in Naïve Bayes Classifier, Bayesian Belief Network: Independence and conditional independence, Use of the Bayesian Belief network in machine learning.

UNIT –III

Supervised learning-Classification: Examples of Supervised Learning, Classification Model, Classification Learning Steps, Common Classification Algorithms: k-Nearest Neighbour(kNN), Decision tree, Random forest model, Support vector machines.

Supervised learning-Regression: Examples of Regression, Common Regression Algorithms: Simple Linear Regression, Multi Linear Regression, Assumptions in Regression Analysis, Main Problems in Regression Analysis, Improving Accuracy of the Linear Regression Model, Polynomial Regression Model, Logistic Regression.

Unsupervised learning: Unsupervised vs Supervised Learning, Application of Unsupervised Learning, Clustering: Clustering as a machine learning task, Different types of clustering techniques, Partitioning methods, k-Medoids : a representative object-based technique, Hierarchical clustering, Density-based methods –DBSCAN, Finding Pattern using Association Rule: Definition of common terms, Association rule, The apriori algorithm for association rule learning, Build the apriori principle rules.

UNIT – IV

Basics of Neural Network: Understanding the Biological Neuron, Exploring the Artificial Neuron, Types of Activation Functions: Identity function, Threshold/step function, ReLU(Rectified Linear Unit) function, Sigmoid function, Hyperbolic tangent function, Early Implementations of ANN: McCulloch-pitts Model of Neuron, Rosenblatts perceptron, ADALINE network model, Architectures of Neural Network: Single-layer feed forward network, Multi-layer feed forward ANNs, Competitive netwok, Recurrent network, Learning Process in ANN:Number of layers, Direction of signal flow, Number of nodes in layers, Weight of interconnection between neurons, Backpropagation Algorithm.

Types of Learning: Representation Learning :Supervised neural networks and multilayer perceptron, Independent component analysis(Unsupervised),Autoencoders, Various forms of clustering, Active Learning: Heuristics for active learning, Active learning query strategies, Instance –Based Learning(Memory- Based Learning): Radial basis function, Pros and cons of instance- based learning method, Association Rule Learning Algorithm: Aprioro algorithm, Eclat algorithm, Ensemble Learning Algorithm: Bootstrap aggregation, Boosting, Gradient boosting machines(GBM), Regularization Algorithm.

UNIT – V

Introduction to Simple Deep Feed forward Neural Network, Hidden Units and their Activation Functions, Architecture Design, Regularization Methods for Deep learning: Early Slopping, Drop out.

Convolutional Neural Networks: Introduction to CNN, Convolution operation, Pooling, Normalization, Application in Computer Vision-Image Net, Sequence Modeling- VGG Net, LeNet.

Recurrent Neural Networks: RNN Topologies, Difficulty in Training RNN, Long Short Term Memory(LSTM):Architecture and Learning Strategy.

TEXT BOOKS:

1.Machine learning by Saikat Dutt, Subramanian Chandramouli, Amit K.Das Pearson Publishers,2019.
2**.** Ian Good fellow, Yoshva Bengio, Aaron Courville, Deep Learning,MIT Press,2016.

REFERENCE BOOKS:

1.Machine learning with python for everyoone by Mark E- Fenner, Pearson Publishers, 2020.
2. Introduction Neural Networks using MATLAB 6.0 – S.N. Shivanandam, S. Sumathi, S. N.Deepa, 1/e, TMH,New Delhi

MIXED SIGNAL DESIGN
(PE – 3)

M.Tech. I Year II-Sem

L	T	P	C
3	0	0	3

Pre-Requisite Analog Electronics

Course Objectives

The objectives of this course are to

1. Introduce circuit design concepts for basic building blocks used in mixed-signal integrated circuit designs.
2. Provide students with the skills to design mixed-signal integrated circuits with these building blocks.
3. Understand design and operation of basic analog circuits.
4. Know mixed signal circuits like DAC, ADC, PLL etc.
5. Design and analysis of switched capacitor circuits
6. Analysis basic data conversion algorithms and circuits.

Course Outcomes

At the completion of this course, each student will have demonstrated proficiency in:

1. Designing CMOS analog circuits to achieve performance specifications.
2. Analyzing CMOS based switched capacitor circuits.
3. Understanding basics of data converters.
4. Understanding mixed-signal design flow.

UNIT I

Switched Capacitor Circuits

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT II

Phased Lock Loop (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT III

Data Converter Fundamentals

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT IV

Nyquist Rate A/D Converters

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT V

Oversampling Converters

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.

TEXT BOOKS

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013.

REFERENCES

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

ADVANCED OPERATING SYSTEMS
(PE -3)

M.Tech. I Year II-Sem

L	T	P	C
3	0	0	3

UNIT I

Introduction to Operating Systems

Overview of computer system hardware, Instruction execution, I/O function, |Interrupts, Memory hierarchy, I/O communication techniques, Operating system objectives and functions, Evaluation of operating system.

UNIT II

Introduction to UNIX and LINUX

Basic commands & command arguments, standard input, output, input / output redirection, filters and editors, Shells and operations.

UNIT III

System Calls

System calls and related file structures, input / output Process creation & termination.

Inter Process Communication

Introduction, file and record locking, Client-Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT IV

Introduction to Distributed Systems

Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems

Layered protocols, ATM networks, Client – Server model, Remote procedure call and Group communicaton.

UNIT V

Synchronization in Distributed Systems

Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions.

Deadlocks

Deadlock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXTBOOKS

1. The Design of the UNIX Operating Systems – Maurice J. Bach, PHI, 1986.
2. Distributed Operating System – Andrew. S. Tanenbaum, PHI, 1994.
3. The Complete reference LINUX – Richard Peterson, 4th Ed., McGraw-Hill.

REFERENCES

1. Operating Systems: Internal and Design Principles – Stallings, 6th Ed., PE.
2. Modern operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles' – Abraham Silberchatz, peter B. Galvin, Greg Gagne,7th Ed., John Wiley.
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming – W. Richard Stevens, PHI, 1998.

WIRELESS SENSOR NETWORKS

(PE-4)

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

Prerequisite: 1.Computer Networks

UNIT 1:

Introduction: Components of a wireless sensor node, Motivation for a Network of Wireless Sensor Nodes, Classification of sensor networks, Characteristics of wireless sensor networks, Challenges of wireless sensor networks, Comparison between wireless sensor networks and wireless mesh networks, Limitations in wireless sensor networks, Design challenges, Hardware architecture, Applications.

Node Architecture: The Sensing Subsystem, the Processor Subsystem, Communication Interfaces, Prototypes.

UNIT –2:

Medium Access Control Protocols for Wireless Sensor Networks

Introduction,Background,Fundamentals of MAC Protocols, Performance Requirements, Common Protocols, MAC Protocols for WSNs, Schedule-Based Protocols, Random Access-Based Protocols, Sensor-MAC Case Study, Protocol Overview, Periodic Listen and Sleep Operations, Schedule Selection and Coordination, Schedule Synchronization, Adaptive Listening, Access Control and Data Exchange, Message Passing, IEEE 802.15.4 LR-WPANs Standard Case Study, PHY Layer, MAC Layer

UNIT – 3:

Routing Protocols for Wireless Sensor Networks

Introduction, Background, Data Dissemination and Gathering, Routing Challenges and Design Issues in Wireless Sensor Networks, Network Scale and Time-Varying Characteristics, Resource Constraints, Sensor Applications Data Models, Routing Strategies in Wireless Sensor Networks, WSN Routing Techniques, Flooding and Its Variants, Sensor Protocols for Information via Negotiation, Low-Energy Adaptive Clustering Hierarchy, Power-Efficient Gathering in Sensor Information Systems, Directed Diffusion, Geographical Routing.

UNIT – 4:

Transport Control Protocols for Wireless Sensor Networks

Traditional Transport Control Protocols, TCP (RFC 793), UDP (RFC 768), Mobile IP, Feasibility of Using TCP or UDP for WSNs, Transport Protocol Design Issues, Examples of Existing Transport Control Protocols, CODA (Congestion Detection and Avoidance), ESRT (Event-to-Sink Reliable Transport), RMST (Reliable Multisegment Transport), PSFQ (Pump Slowly, Fetch Quickly), GARUDA, ATP (Ad Hoc Transport Protocol), Problems with Transport Control Protocols, Performance of Transport Control Protocols, Congestion, Packet Loss Recovery.

UNIT – 5:

Node and Network Management: Power Management, Local Power Management aspects, Dynamic Power Management, Conceptual Architecture.

Time Synchronization: Clocks and the Synchronization Problem, Time Synchronization in Wireless Sensor Networks, Basics of Time Synchronization, Time Synchronization Protocols.

Localization: Ranging Techniques, Range-Based Localization, Range-Free Localization, Event- Driven Localization.

TEXT BOOKS:

1. WaltenegusDargie, Christian Poellabauer, "Fundamentals of Wireless Sensor Networks: Theory and Practice", Wiley 2010.
2. Kazem Sohraby, Daniel Minoli ,Taieb Znati," Wireless Sensor Networks, Technology, Protocols, and Applications" Wiley 2007
3. Mohammad S. Obaidat, SudipMisra, "Principles of Wireless Sensor Networks", Cambridge, 2014.
4. Holger Karl, Andreas Willig, "Protocols and Architectures for wireless sensor networks" Wiley, 2005.

REFERENCE BOOKS:

1. Ian F. Akyildiz, Mehmet Can Vuran , "Wireless Sensor Networks", Wiley, 2010.
2. C.S. Raghavendra, K.M. Sivalingam, TaiebZnati, "Wireless Sensor Networks", Springer, 2010
3. C. Sivarammurthy& B.S. Manoj, "Adhoc Wireless Networks",1st Edition, PHI,2004.
4. Fei Hu., Xiaojun Cao, "Wireless Sensor Networks",1st Edition, CRC Press, 2013.
5. Carlos de MoraisCordeiro&DharmaprakashAgarwal," Adhoc& wireless sensor, 2nd edition, World Scientific & Imperial college press, 2006.
6. Sunil Kumar, S. Manvi, Mahabalaseshwar, "Wireless & sensor mobile networks concepts and protocols" Wiley, 2010.

ARTIFICIAL NEURAL NETWORKS & DEEP LEARNING

(PE-4)

M.Tech. I Year II-Semester

L	T	P	C
3	0	0	3

UNIT-I :

Fundamental Concepts, Models & Learning Rules of Artificial Neural Systems

Artificial Neuron Models: Biological Neuron, Mcculloch-pitts Neuron Model, Activation Functions, Boltzman Neuron Model, Models of Artificial Neural Networks : Feed forward Network, Feedback Network, Neural Processing, Learning and Adaption : Supervised, Unsupervised and Reinforcement Learning.

Neural Network Learning Rules: Hebbian Learning Rule, Perception Learning Rule, Delta Learning Rule Widrow –Hoff Rule, Correlation Learning Rule, Winner –Take – All Learning Rule, Outstar Learning Rule, Summary of Learning Rules.

Single Layer Feed Forward Networks:

Classification Model, Features and Decision Regions, Discriminant Functions, linear Machine and Minimum Distance Classification, Non – Parametric Training Concept, Training and Classification Using the Discrete Perceptron: Algorithm and Examples. Single Layer Continuous Perceptron Networks for Linearly Separable Classification, Perceptron Convergence Theorem, Multi Category Single Layer Perceptron Networks.

UNIT –II

Multi Layer Feed Forward Networks:

Linearly Non- Separable, Pattern Classification, Delta Learning Rule for Multi Perception, Generalized Delta Learning Rule. Feed Forward Recall and Error Back Propagation Training ; Examples of Error Back Propagation, Training Errors, Learning Factors ; Initial Weights Cumulative Weight Adjustment Versus Incremental Updating, Steepness of Activation Function, Learning Constant, Momentum Method, Network Architecture Versus Data Representation, Necessary Number of Hidden Neurons. Application of Back Propagation Networks in Pattern Recognition and Image Processing.

UNIT –III :

Associative Memories:

Basic Concepts of Linear Associative, Basic Concepts of Dynamical Systems, Mathematical Foundation of Discrete Time Hop field Networks. Mathematical Foundation of Gradient- Type Hop Field Networks, Transient Response of Continuous Time Networks, Example Solution of Optimization Problems; Summing Networks with Digital Outputs, Minimization of the Traveling salesman tour length, Solving Simultaneous Linear Equations, Boltzman machines, Bidirectional Associative Memory; Multidirectional Associative Memory, Associative Memory of Spatio-temporal Patterns.

UNIT – IV :

Matching and Self-Organizing Networks:

Hamming net and MAXNET Unsupervised learning of clusters, Clustering and similarity measures Winner take all learning, recall mode, initializing of weights, separability limitations, Counter propagation networks, Feature mapping: Self organizing feature maps, Cluster discovery networks (ART1).

UNIT – V :

Introduction to Simple Deep Feed forward Neural Network, Hidden Units and their Activation Functions, Architecture Design, Regularization Methods for Deep learning: Early Slopping, Drop out.

Convolutional Neural Networks: Introduction to CNN, Convolution operation, Pooling, Normalization, Application in Computer Vision-Image Net, Sequence Modeling- VGG Net, LeNet.

Recurrent Neural Networks: RNN Topologies, Difficulty in Training RNN, Long Short Term Memory(LSTM):Architecture and Learning Strategy.

TEXT BOOKS:

1. Introduction to Artificial Neural Systems – J.M.Zurada, Jaico Publishers.
2. Ian Good fellow, Yoshva Bengio, Aaron Courville, Deep Learning,MIT Press,2016.
3. Introduction Neural Networks using MATLAB 6.0 – S.N. Shivanandam, S. Sumathi, S. N.Deepa, 1/e, TMH,New Delhi

REFERENCE BOOKS:

1. Elements of Artificial Neural Networks – Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International.
2. Artificial Neural Network – Simon Haykin,2nd Ed., Pearson Education
3. Artificial Neural Networks – Dr.B. Yagananarayana, 1999,PHI, New Delhi.
4. Fundamental of Neural Networks- Laurene Fausett.

COMMUNICATION AND NETWORK TECHNOLOGIES FOR IOT

(PE-4)

M.Tech. I Year II-Sem

L	T	P	C
3	0	0	3

UNIT-I

Introduction to IoT

Flavor of the Internet of Things, Technology of the Internet of Things & Enchanted Objects, Design Principles for Connected Devices, Calm and Ambient Technology, Web Thinking for Connected Devices, First-Class Citizens On The Internet, Thinking About Prototyping, Sketching, Familiarity, Prototypes and Production, Open Source versus Closed Source, Closed Source for Mass Market Projects, Tapping into the Community.

UNIT-II

IoT Paradigm,

Why the IoT Is Strategically Sound, Brewing and Blossoming Trends in IT Space, Envisioning the Internet of Things Era, Device-to-Device/Machine-to-Machine Integration Concept, Explaining the Aspect of Device-to-Cloud (D2C) Integration, Describing the Sensor-to-Cloud Integration Concept, Emerging IoT Flavors, Prominent IoT Realization Technologies, Cloud-to-Cloud (C2C) Integration, and Device-to-Cloud (D2C) Integration.

UNIT-III

Wireless Technologies for IoT Ecosystem

Introduction, Architecture for IoT Using Mobile Devices, Mobile Technologies for Supporting IoT Ecosystem, Energy Harvesting for Power Conservation in the IoT System, Mobile Application Development Platforms and Use of IoT, Low Power Wide Area Networking Technologies, Direct & Indirect Device Connectivity Topology of LPWAN, LoRa WaN.

UNIT-IV

Protocols for the IoT Ecosystem

Introduction, Layered Architecture for IoT, Protocol Architecture of IoT, Routing Protocol, IEEE 802.15.4, Bluetooth Low Energy, ZigBee, Protocols for IoT Service Discovery, Prominent IoT Service Discovery Products, IP Addresses, Infrastructure Protocols, Static IP Address Assignment, Dynamic IP Address Assignment, IPV6, TCP and UDP Ports, Application Layer Protocols.

Enablement Platforms for IoT Applications

IoT Building Blocks, IoT or Sensor Data Gateway, Application Enablement Platforms, IoT Application Enablement Platforms, IoT and M2M Sensor Data Platform, IoT Data Analytics Platforms, IoT Data Virtualization Platforms, IoT Edge Data Analytics.

UNIT-V
Integration Technologies of IoT

Introduction, IoT Portion for Smarter Enterprises and Environments, Sensor and Actuator Networks, IoT Device Integration Concepts, Device Profile for Web Services, Open Service Gateway, Scalability, Robustness, openHAB, Remote OSGi, Device Integration Protocols and Middleware, Data Distribution Bus, Message Queue Telemetry Transport, Extensible Messaging and Presence Protocol, Protocol Landscape for IoT.

Smart Use Cases of IoT
Introduction, Collaboration Platforms, Geospatial Platforms, Open Access to Public Data, Smart Industrial Use Cases of IoT, Smart Lighting for Energy Conservation, Smart Transportation Systems, Smart Homes/Buildings, Smarter Homes—Middleware Platforms, Smart Education Systems Using Wearable Devices

Text Books

1. "The Internet of Things Enabling, Technologies, Platforms and Applications" by Pethuru Raj and Anupama C.Raman CRC Press Taylor & Francis Group.
2. "Designing the Internet of Things " by Adrain McEwen , Hakim Cassimally Wiley 1st Edition

VLSI SIGNAL PROCESSING
(PE-4)

M.Tech. I Year II-Sem

L	T	P	C
3	0	0	3

Prerequisite: VLSI Technology, Digital Signal Processing

Course Objectives

The objectives of this course are to:

1. Introduce techniques for the existing DSP structures to suit VLSI implementations.
2. Introduce efficient design of DSP architectures suitable for VLSI.
3. Understand various fast convolution techniques.
4. Understand low power processors for signal processing and wireless applications

Course Outcomes

On successful completion of the module, students will be able to:

1. Ability to modify the existing or new DSP architectures suitable for VLSI.
2. Understand the concepts of folding and unfolding algorithms and applications.
3. Ability to implement fast convolution algorithms.
4. Low power design aspects of processors for signal processing and wireless applications.

UNIT -I

Introduction to DSP

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

Pipelining and Parallel Processing

Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power

Retiming

Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT –II

Folding and Unfolding

Folding- Introduction, Folding Transform, Register minimization Techniques, Registerminimization in folded architectures, folding of Multirate systems

Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT -III

Systolic Architecture Design

Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT -IV

Fast Convolution

Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT -V

Low Power Design

Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, PowerEstimation Approaches

Programmable DSP

Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parthi, Wiley Inter Science, 1998.
2. VLSI and Modern Signal processing – Kung S. Y, H. J. While House, T. Kailath, Prentice Hall, 1985.

REFERENCES

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
2. VLSI Digital Signal Processing – Medisetti V. K, IEEE Press (NY), 1995.

FPGA DESIGN LAB

M.Tech. I Year II-Semester

L	T	P	C
0	0	4	2

Design, Simulate, Synthesize the following circuits targeting 7 series FPGA

1. 8-bit-bit low power high speed adder a. Carry save adder b. Carry skip adder
2. High Speed and low power 16/32/64-bit adder using an 8-bit adder
3. 8x8 Braun multiplier
4. 16x16 bit multiplier using IP Core.
5. A Clock divider
6. FIFO using IP core
7. 8 bit ALU
8. Circular Buffer
9. 2D RAM Array
10. Implement MAC unit targeting Artix 7 FPGA employing low power techniques while meeting target speed

ANALOG AND DIGITAL IC DESIGN LAB

M.Tech. I Year II-Semester

L	T	P	C
0	0	4	2

Design and simulate the following circuits:

1) Design and simulate the basic current sink
2) Design and simulate the Bootstrap current sink
3) Design and simulate the Transconductance analysis
4) Design and simulate the current source
5) Design and simulate the current mirror
6) Design and simulate the differential amplifer
7) Design and simulate the cascade current source
8) Design and simulate the cascade amplifier
9) Design CMOS inverter and plot its static and dynamic characteristics
10) Design the Universal NAND/NOR gates.
11) Design of Flip flops
12) Design Adder circuit using NAND/NOR gates.
13) Design Multiplier using NAND/NOR gates.
14) Design Shit registers using Flip flops.
15) Design memory circuits using SRAM / DRAM

VALUE EDUCATION
(AUDIT COURSE-II)

M.Tech. I Year II-Semester

L	T	P	C
2	0	0	0

Course Objectives: To help the students:
1. Understand value of education and self- development
2. Imbibe good values
3. Know about the importance of character

Course outcomes: Students will be able to:
1. Acquire knowledge about self-development
2. Learn the importance of Human values
3. Develop the overall personality

Syllabus

Unit1
Values and Self-development – Social Values and Individual Attitudes. Work Ethics, Indian Vision of Humanism. Ethical Standards and Principles. Value Judgments

Unit2
Importance of Cultivating Values. Sense of Duty. Devotion, Self-reliance, Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. National Unity. Patriotism. Love for Nature, Discipline

Unit 3
Personality and Behavior Development - Soul and Scientific Attitude- Integrity and Discipline. Punctuality- Compassion and Benevolence - Positive Thinking- Composure and Equipoise- Dignity of Labour. Universal Brotherhood and Religious Tolerance. True Friendship. Happiness Vs Suffering- Aware of Self-destructive Habits. Association and Cooperation. Eco-friendly Consciousness

Unit4
Character and Competence – Values of Scriptures- Self-management and Good health. Science of Reincarnation. Equality, Nonviolence, Humility, Role of Women- Secular Thinking- Mind your Mind, Self-control- Non Ethnocentric Behavior

Suggested Readings

1. Chakroborty, S.K. "*Values and Ethics for organizations Theory and practice*", Oxford University Press, New Delhi. 1998.
2. Dostoyevsky, Fyodor, Constance Garnett, and Ernest J. Simmons. *Crime and Punishment*. New York: Modern Library, 1950. Print.
3. Galsworthy, John. *Justice***.** Czechia, Good Press, 2019.
4. TED Talks

****

HARDWARE AND SOFTWARE CO-DESIGN
(PE-5)

M.Tech. II Year I-Semester

L	T	P	C
3	0	0	3

Prerequisite: Advanced Computer Architecture, Embedded System Design**.**

Course Objective:

1. To provide a broad understanding of the specific requirement of Hardware and soft ware integration for embedded system

Course Outcomes:

1. To acquire the knowledge on various models
2. To explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools
4. Understand validation methods and adaptability.

UNIT –I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co- Synthesis Algorithms:** Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT –II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent
computations, interfacing components, design verification, implementation verification, verificationtools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level
specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, KluwerAcademic Publishers

REFERENCES

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

SYSTEM DESIGN ASPECTS OF IOT

(PE-5)

M.Tech. II Year I-Semester

L	T	P	C
3	0	0	3

Pre-requisite:

Course Objectives

The objectives of the course are to

1. Understand the concepts of Internet of Things and able to build IoT applications.
2. Learn the programming and use of Arduino and Raspberry Pi boards.
3. Known about data handling and analytics in SDN.

Course Outcomes

Upon completing this course, the student will be able to

1. Known basic protocols in sensor networks.
2. Program and configure Arduino boards for various designs.
3. Python programming and interfacing for Raspberry Pi.
4. Design IoT applications in different domains.

UNIT I

Definition and Characteristics of IoT, Physical Design of IoT: Things in IOT, IOT Protocols, Logical Design of IoT: IOT functional Blocks, Communication Models, Communication APIs, IOT levels and deployment templates, Sensor Networks, Sensors and Actuators, ADCs and DACs

Machine-to-Machine Communications, Difference between IoT and M2M, Interoperability in IoT, Software defined Network (SDN) and NFV for IoT

UNIT II

Domain Specific IOTs

Home Automation: Smart Lighting, Smart Appliances, Intrusion Detection, Smoke/ Gas detector; Smart Cities: Smart Parking, Smart Lighting,Smart Roads, Structural Health Monitoring, Surveillance, Emergency Response, Environment: Weather Monitoring, Air Pollution Monitoring, Noise Pollution Monitoring, Forest Fire Detection, River Floods Detection, Energy: Smart Grids, Renewable Energy Systems, Prognostics, Retail: Inventory Management, Smart Payments, Smart Vending Machines, Logistics: Route Generation and Scheduling, Fleet Tracking, Shipment Monitoring, Remote Vehicle Diagnostics, Agriculture: Smart Irrigation, Green House Control, Industry: Machine Diagnosis and Prognosis, Indoor Air Quality Monitor, Health and Life Style: Health and Fitness Monitoring, Wearable Electronics.

UNIT III

Arduino and IOT:

Introduction XBee module, Interfacing with XBee, Pin diagram, updating Firmware: AT Commands and API, Configuring XBee as Coordinator, Router, Building an XBee-ZB Mesh Network and Testing.

Arduino Programming: Arduino models and Clones,Arduino IDE, Integration of Sensors and Actuators with Arduino :Sketch for blinking of LED, Building an Aurdino Temperature and Humidity Sensor,Using an Arduino as a Data Collector for XBee Sensor Nodes

UNIT IV

Applied Python Programming with Raspberry Pi: Introduction to Python programming, Introduction to Raspberry Pi modules, Installing a Boot image in Pi, GPIO pins of Pi, Sketch for blinking of LED using Pi, Building an Raspberry Pi Temperature and Humidity Sensor,Building a Raspberry Barometric Pressure Sensor Node, Creating a Raspberry Pi Data Collector for XBee Sensor Nodes,

UNIT V

Data Analytics for IOT

Apache Hadoop: Map Reduce Programming Model, Hadoop Map Reduce Job Execution, Map Reduce Job Execution Workflow, Hadoop Cluster Setup, Using Hadoop MapReduce for Batch Data Analysis: Hadoop YARN, Apache Oozie: Setting up Oozie, Oozie Workflows for IoT Data Analysis, Apache Spark, Apache Storm : Setting up a Storm Cluster, Using Apache Storm for Real-time Data Analysis: REST-Based approach, WebSocket-based Approach.

TEXT BOOKS

1. Internet of Things: A Hands-on Approach, by ArshdeepBahga and Vijay Madisetti.
2. Beginning Sensor networks with Arduino and Raspberry Pi – Charles Bell, Apress, 2013.

REFERENCES

1. The Internet of Things: Enabling Technologies, Platforms, and Use Cases, by Pethuru Raj and Anupama C. Raman (CRC Press)
2. Fundamentals of Wireless Sensor Networks: Theory and Practice - WaltenegusDargie, Christian Poellabauer.
3. Make sensors: Terokarvinen, kemo, karvinen and villeyvaltokari, 1st Ed., MakerMedia, 2014.

AD-HOC AND WIRELESS SENSOR NETWORKS

(PE-5)

M.Tech. II Year I-Semester	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

Prerequisite: Wireless Sensor Networks

Course Objectives

The objectives of this course are to make the student
1. To study the fundamentals of WLANs & WPANs.
2. To study the fundamentals of wireless Ad-Hoc Networks.
3. To study the operation and performance of various Ad-Hoc wireless network protocols.
4. To study the architecture and protocols of Wireless sensor networks.

Course Outcomes

On completion of this course student will be able to
1. Understand the design issues, protocol architecture and functions of various protocols of WLANs & WPANs.
2. Understand the design issues of Ad-Hoc networks and operation of MAC, routing and transport protocols.
3. Analyze and compare various MAC protocols, Routing protocols and transport layer protocols of Ad-Hoc networks.
4. Understand various sensor network architectures, data dissemination and data gathering methods

UNIT I

Wireless LANs and PANs

Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.

AD HOC WIRELESS NETWORKS

Introduction, Issues in Ad Hoc Wireless Networks.

UNIT II

MAC Protocols

Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention-Based Protocols, Contention-Based Protocols with reservation Mechanisms, Contention–Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT III

Routing Protocols

Introduction, Issues in Designing a Routing Protocol for Ad-Hoc Wireless Networks, Classification of Routing Protocols, Table–Driven Routing Protocols, On–Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power–Aware Routing Protocols.

UNIT IV

Transport Layer Protocols

Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT V

Wireless Sensor Networks

Introduction, Sensor Network Architecture-Layered Architecture, Clustered Architecture, Data Dissemination-Flooding, Gossiping, Rumor Routing, Sequential Assignment Routing, Directed Diffusion, Sensor Protocols for Information via Negotiation, Cost Field Approach, Geographic Hash Table, Small Minimum Energy Communication Network, Data Gathering-Direct Transmission, Power Efficient Gathering for Sensor Information Systems, Binary Scheme, Chain based Three Level Binary Scheme, MAC Protocols for Sensor Networks-Self Organizing MAC for Sensor Networks and Eavesdrop and register, Hybrid TDMA/FDMA, CSMA based MAC protocols, Location Discovery-Indoor localization, Sensor network localization, Quality of a Sensor Network- Coverage, Exposure, Evolving Standards.

TEXT BOOKS

1. Ad Hoc Wireless Networks Architectures and Protocols C. Siva Ram Murthy B.S. Manoj, Prentice Hall, 6th Edition, 2008.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.

REFERENCES

1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C.K. Toh , 1st Ed. Pearson Education.
2. Ad Hoc and Sensor Networks Theory and Appications- Carols de Morais Cordeiro and Dharma prakash Agrawal, World Scientific

3. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer

ALGORITHMS FOR VLSI DESIGN
(PE - 5)

M.Tech. II Year I-Sem

L	T	P	C
4	0	0	4

Pre-Requisite: VLSI

Course Objectives

The objectives of this course are to:
1. To provide knowledge on broad spectrum of issues related to design automation of VLSI circuits.
2. To provide exposure to various tools and their applications in design automation.

Course Outcomes

On completion of this course the student will be able to:
1. Expected to learn graph theory and its applications.
2. Understand the methods of combinational circuit optimization.
3. Expose design automation using FPGA.
4. Capable to physical design automation of MCMs.

UNIT I

PRELIMINARIES

Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION

Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING

Problems, Concepts and Algorithms. MODELLING AND SIMULATION
Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT IV

LOGIC SYNTHESIS AND VERIFICATION

Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis
HIGH-LEVEL SYNTHESIS, Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGAs

FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs

MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.1999.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed.,Springer International Edition, 2005.

REFERENCES

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson,Wiley, 1993.
2. Modern VLSI Design :Systems on silicon – Wayne Wolf, 2nd Ed., Pearson Education Asia, 1998.

PRINCIPLES OF SIGNAL PROCESSING
(OE)

M.Tech. II Year I-Sem

L	T	P	C
3	0	0	3

Course Objectives

1. This gives the basics of Signals and Systems required for all Engineering related courses.
2. To understand the basic characteristics of LTI systems.
3. To know the signal transmission requirements.
4. This gives basic understanding of signal statistical properties and noise source concepts.

Course Outcomes

Upon completing this course, the student will be able to

1. Differentiate various signal functions.
2. Understand the characteristics of linear time invariant systems.
3. Understand the concepts sampling theorem.
4. Determine the Spectral and temporal characteristics of Signals.
5. Understand the concepts of Noise in Communication systems.

UNIT I

Signal Analysis

Analogy between Vectors and Signals, Orthogonal Signal Space, Signal approximation using Orthogonal functions, Mean Square Error, Closed or complete set of Orthogonal functions, Orthogonality in Complex functions, Classification of Signals and systems, Exponential and Sinusoidal signals, Concepts of Impulse function, Unit Step function, Signum function.

UNIT II

Signal Transmission through Linear Systems

Linear System, Impulse response, Response of a Linear System, Linear Time Invariant(LTI) System, Linear Time Variant (LTV) System, Transfer function of a LTI System, Filter characteristic of Linear System, Distortion less transmission through a system, Signal bandwidth, System Bandwidth, Ideal LPF, HPF, and BPF characteristics, Convolution and Correlation of Signals, Concept of convolution in Time domain and Frequency domain, Graphical representation of Convolution.

UNIT III

Sampling Theorem

Graphical and analytical proof for Band Limited Signals, Impulse Sampling, Natural and Flat top Sampling, Reconstruction of signal from its samples, Effect of under sampling – Aliasing, Introduction to Band Pass Sampling.

UNIT IV

Temporal characteristics of signals

Concept of Stationarity and Statistical Independence. First-Order Stationary Processes, Time Averages and Ergodicity, Cross Correlation and Auto Correlation of Functions, Properties of Correlation

Functions, Cross-Correlation Function and Its Properties. Power Spectrum and its Properties, Relationship between Power Spectrum and Autocorrelation Function.

UNIT V

Noise sources

Resistive/Thermal Noise Source, Arbitrary Noise Sources, Effective Noise Temperature, Noise equivalent bandwidth, Average Noise Figures, Average Noise Figure of cascaded networks, Narrow Band noise, Quadrature representation of narrow band noise & its properties.

TEXT BOOKS

1. Signals, Systems & Communications - B.P. Lathi , B.S. Publications, 2013.
2. Probability, Random Variables & Random Signal Principles - Peyton Z. Peebles, TMH, 4th Edition, 2001.

REFERENCES

1. Signals and Systems - A.V. Oppenheim, A.S. Willsky and S.H. Nawabi, 2 Ed.
2. Fundamentals of Signals and Systems - Michel J. Robert, 2008, MGH International Edition.
3. Random Processes for Engineers-Bruce Hajck, Cambridge unipress,2015
4. Statistical Theory of Communication – S.P Eugene Xavier, New Age Publications, 2003.