Dr. M AshaRani

PhD in Faculty of ECE, M.Tech Digital Systems & Computer Electronics, B.E ECE

Senior Professor

Electronics & Communication Engineering

Areas of Interest:
Digital System Design, Design of Fault Tolerant Systems, Microprocessor & Microcontrollers, VLSI Design & Embeded Systems.

Submitted Ph.D Thesis on "Design of Built in self Test and repair scheme for static RAMs". Published 6 technical papers in National & International Conferences. Co-ordinated one TAPTEC project of Rs.6.50 Lakhs in establishing VLSI Lab and one R&D project of Rs. 9.0 Lakhs in designing an ASIP for Image Processing applications sponserd by AICTE, Delhi, Co-ordinator for SPOORTHI' 04 a student symposium.
Co-ordinatd 4 Refresher Courses conducted by Acad. Staff College, JNTU Hyderabad. Attended about 10 workshops on VLSI -EDA Tools, Design for Testability, Altera-Tools, SILVACO tools, National Instruments - Virtual Instruments - Lab view etc.

Contact :

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