CURRICULUM VITAE

(Vi) J.P.Gudem, Mdl: Chilukuru,
Dist: Nalgonda,
Status: Single

NARENDER REDDY KAMPELLI,
E-mail:narenderreddy.kampelli@gmail.com,
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CAREER OBJECTIVE

I am aspiring to build a career in the teaching profession with a leading educational institution that will explore my teaching abilities and establish myself as a good researcher and teacher.

EXPERTISE

Hands-on Experience in Partitioning and synthesis of **SOC RTL** for **Xilinx Vertex 5** Mapping, placement, and Routing using **ISE 10.1**

Full Custom Design using Cadence Tool

Network Simulator Tool

EDUCATIONAL QUALIFICATIONS

- ✓ Pursuing Ph.D from JNT University Hyderabad
- ✓ **M.Tech** in VLSI System Design from **CVR College of Engineering** JNTUH, Hyderabad, AP with **71.75%** in 2011.
- ✓ **B.E**. in Electronics and Communication Engineering from **M.V.S.R. Engineering College**, Hyderabad, AP with 65.52%in 2006.
- ✓ **Intermediate** from Nalanda Residential Junior College, Vijayawada, AP with **93.7%**
- ✓ **CBSE** from Jawahar Navodaya Vidyalaya, Chalakurthy camp, Nalgonda (Dist.) AP with 81.2%.

EXPERIENCE.

- ✓ Worked as Asst. Professor in ECE department in Bharat Institute of Engineering and Technology, Hyderabad from July 2006 – May 2007.
- ✓ Worked as Asst. Professor in ECE department in Madhira Institute of Technology & Sciences, Kodad, Nalgonda (Dist.) from June 2008 – June 2009.
- ✓ Worked as Asst. Professor in ECE department in Bharat Institute of Engineering and Technology, Hyderabad from Jun 2012 – April 2013.
- ✓ Worked as Asst. Professor in ECE department in CMR Institute of Technology Medchal, Hyderabad from June 2013 –June,2 14
- ✓ Working as Asst. Professor(Contract) in ECE Department Since July, 14 to date in JNTUH College of Engineering Hyderabad, Kukatpally, JNTUH

SOFTWARE EXPOSURE

- ✓ **Hardware Description Languages** Verilog, Fundamentals of VHDL.
- ✓ **EDA Tools**
- ✓ Xilinx *ISE v 10.1i*
- ✓ Mentor Graphics *Model Sim v 6.1*
- ✓ Cadence *Virtuoso* bundle of tools,

PROJECTS

M.Tech. ***Major Project***

Project Title: **Design of VCO-based ADC in 180nm CMOS Process**

Duration: **Oct 2010 to Dec 2011**

Location: CVR College of Engineering, Hyderabad.

Team: One

Responsibilities: Design of different modules in Full Custom Using Cadence ICFB tool in .18 **µm** CMOS Process.

B. E. **Major Project**

Project Title: ***Simulation of various modules of Micro-Controller using VHDL***

Duration: **December 2005 to May 2006** (Six Months)

Location: M.V.S.R Engineering College, Hyderabad.

Team: Three

Role: Project Leader

Responsibilities: VHDL Coding of the modules of the Micro-Controller are done. With the simulation, functioning is verified. For Synthesis Xilinx's ISE 6.2i is used.

PROFESSIONAL ACTIVITIES

- ➢ In charge, of **IETE** in Madhira Institute of Technology & Sciences, Kodad.

MEMBERSHIP IN PROFESSIONAL BODIES

- ➢ Member, Indian Society for Technical Education (**ISTE**)

ACTIVITIES

- Participated in **International Student conference on VLSI Design & Embedded systems** 9th and 10th January, 2012.
- Participated in the RASDAT-2012, 3rd IEEE International Workshop on **Reliability Aware System Design and Test** In conjunction with the 25th International Conference on VLSI Design at Hyderabad, India January 7-8, 2012.
- Participated in the joint workshop organized by JNTUH, Mentor Graphics Corp., & Trident Techlabs on '**VLSI Design Methodology Using Mentor Graphics Tools'** held on August 9th -13th, 2010 at Hyderabad.
- Attended a tutorial titled **Advanced-Mixed Signal System and Circuit Techniques** at the 24th International Conference on VLSI Design held at IIT Madras, Chennai, during January 2-7, 2011.
- Participated in the 'Two Days Workshop on **VLSI Design Using Xilinx Tools** (Theory & Practice)' held at CVR College of Engineering, Hyderabad, during December 2-3,2010.
- Presented poster on **ULSI** in SINCHRONISM-2005, A State Level Student Technical Symposium held at MVSR Engineering College, Hyderabad in February 2005
- Participated in 3rd National Seminar on **"e-Learning & e-Learning Technologies"** ELELTECH INDIA 2009 organized by C-DAC, Hyderabad and JNT University Hyderabad in Association with DIT, MCIT held during November 5-6, 2009 at JNTUH, Hyderabad.

Achievements

- ✓ Selected for the Jawahar Navodaya Vidyalaya Chalkurthy Camp, Nalgonda District Wise Test for 6th to 12th class admission in 1996.
- ✓ Stood in **first place** in Intermediate in my College and got a **617** rank in **EAMCET 2002**
- ✓ Stood **3rd** and **11th** in **PGECET_2009** ranking in Embedded Systems, ECE examination respectively.
- ✓ Qualified for **GATE-2013**, obtained a score of **381**
- ✓ Qualified for UGC-**NET** Assistant **Professorship** held on Dec-29,2014

AREAS OF INTEREST

- Wireless Communication Networks
- Electro Magnetic Fields and Waves
- VLSI System Design

COURSES TAUGHT:

- Principles of Electrical Engineering
- Electronic Devices & Circuits
- Electro Magnetic Waves & Transmission Lines
- Digital Electronics
- Electronic Circuit Analysis
- VLSI Design
- Network Analysis & Transmission Lines
- Microwave Engineering
- Electromagnetic Fields & Waves
- Antennas & Wave Propagation
- Advanced Data Communication
- 4G Technology
- Analog Communication

PERSONAL DETAILS

Father's Name**:** Venkata Reddy

Age & DOB**:** 39 years, 16-09-1983

Sex**:** Male.

Marital Status**:** Single

Nationality**:** Indian

Languages Known**:** English, Hindi, and Telugu

Hobbies**:** Reading Articles on Current Trends, Blogging, and Counselling

Permanent Address : village: Jerripothula Gudem
Mandal: Chilukuru
District: Suryapet

I, Narender Reddy Kampelli, declare that the above-written particulars are the best of my knowledge.

Date: 16-06-2023

Hyderabad **(NARENDER REDDY KAMPELLI)**