

CURRICULAM VITAE

Devisingh

s/o R.Budhyanayak
H.No:3-48, Kishan Naik Thanda,
Wasar(village),
Kangti(mdl),
Medak(dist),
Telangana,India 502286

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Career Goal

To achieve responsible position, that gives me scope to apply my knowledge and skills in the advanced technologies and be a part of team, which dynamically works towards success and growth of the organization.

Educational Qualification

Standard/Degree	Year	College/School	% Marks
M.Tech (IC Technology)	2011-2013	University of Hyderabad	7.76(CGPA)
B.Tech(electronics &communication engg)	2006-2010	Padmasri DR BV Raju Institute Of Technology ,Narsapur,Medak, AP	62.72
Senior Sec (+2)	2006	Dr BR A C Social Welfare Residential Jr college,Hathnoora,Medak,AP	81
Secondary(10th)	2004	AP Social Welfare Residential boys school,Nallavagu,Medak,AP	86.8

Teaching experience:-

- 1.Currently Working as a Assistant Professor(C) in the Electronics and Communication Engineering Department at JNTUHUCES, Sultanpur, from September, 2015
2. I worked From 18-12-2014 to 27-06-2015 as **Assistant Professor** in MLRITM, Dundigal.

3. I worked From 10-01-2014 to 15-12-2014 as **Assistant Professor** in Mallareddy engineering and management sciences medchal.

Academic Activities:-

1. Presented the paper in online mode titled “ Navigating the Bio-Digital Revolution: AI's Role in Achieving Sustainable Development Goals” in the "International Conference on Next Generation Communication & Information Processing (INCIP 2025)" held on January 23 to January 24, 2025.organized by Manipal Institute of Technology, Bengaluru.
2. Presented the paper in online mode titled “AI and ML Strategies for Robust Beam Management in 5G Systems” in the "International Conference on Next Generation Communication & Information Processing (INCIP 2025)" held on January 23 to January 24, 2025.organized by Manipal Institute of Technology, Bengaluru.
3. Received appreciation certificate as a Reviewer for the IEEE "International Conference on Next Generation Communication & Information Processing (INCIP 2025)" organized by Manipal Institute of Technology, Bengaluru, from January 23 to January 24, 2025.
4. Participated in Online"Faculty Induction Programme" held from 28/06/2021 to 04/08/2021 and successfully completed with A Grade

NPTEL Online Certification Funded By Ministry Of HRD Govt. Of India Successfully

Completed Courses:-

1. Digital circuits
2. Analog circuits
3. Digital System Design

Published papers:-

1. Adavathu Rajitha and Devisingh “A LOW-POWER HIGH-SPEED ACCURACY CONTROLLABLE APPROXIMATE MULTIPLIER DESIGN” ijesat Vol 25 Issue 07, pages 102-109 ,July, 2025
2. Kondeti Chirunadh and Devisingh “VLSI ARCHITECTURE FOR DATA TRANSMISSION EFFICIENCY IN WSNs: INTEGRATING BAQ AND LEACH PROTOCOL STRATEGIES” Industrial Engineering Journal Volume : 54, Issue 7, pages 812-818 ,July : 2025.
3. K. Aravinda, Tejaswini Rangaraju,Atul Singla, Ashish Parmar,Sajjad Ziara and Devisingh“Navigating the Bio-Digital Revolution: AI's Role in Achieving Sustainable Development Goals” Published in: 2025 International Conference on Next Generation Communication & Information Processing (INCIP), 23-24 January 2025 , Page(s):262 - 267,published on 09 June 2025
DOI: 10.1109/INCIP64058.2025.11019665
4. V. Asha,Yagateela Pandu Rangaiah,Ginni Nijhawan,Abhishek Kaushik,Ali Albawi and Devisingh “AI and ML Strategies for Robust Beam Management in 5G Systems”Published in: 2025 International Conference on Next Generation Communication & Information Processing (INCIP), 23-24 January 2025 , Page(s):274 - 280,published on 09 June 2025.
DOI: 10.1109/INCIP64058.2025.11019161
5. Macherla Jeevani, Devisingh, and Talari Mohan Das “Effective design and implementation of polar code decoding and encoding with successive cancellation”Industrial Engineering Journal Volume : 53, Issue 8, pages 81-92 ,August : 2024.
6. Peddi Chandrakiran, Devisingh And K Prabhu“A NOVEL TO ADDRESS DOUBLE BIT ERRORS IN SRAM BASED EMULATED TCAMS” Industrial Engineering Journal Volume : 53, Issue 8, pages 83-80, August : 2024
7. Devisingh, M.Anil Kumar and C. Laxmi Prasad “DCT-PCA Based automatic facial expression recognition using facial patches” Volume 06, Issue 01, Pages: 34-42 Jan 2017.
8. Devisingh, M.Anil Kumar and C. Laxmi Prasad “Data encoding and decoding techniques for reducing energy consumption” Volume 05, Issue 03, Pages: 21-28, Mar 2016.

9. Devisingh “realization of BIST architecture using SRAM cell based on input vector monitoring” IJECEC ,VOLUME1 ISSUE 4, Pages: 16-21, July 2015.

Responsibility:-

1. Appointed as Local Route Officer for Group III Examination–2024 Telangana Public Service Commission Government of Telangana at Sangareddy dated 17and 18 November 2024.
2. Appointed as Observer for TS EAPCET – 2024 on 07/05/2024 to 10/05/2024 Hyderabad Institute of Technology and Management, Hyderabad.
3. Appointed as evaluator for various B.Tech ECE subjects Spot Valuation at University Examination Branch Jawaharlal Nehru Technological University Hyderabad

AREAS OF INTEREST

Semiconductor Device Fabrication
Semiconductor Device Characterization
Digital And Analog VLSI Design
Digital Electronics

Strengths

- Highly motivated and adaptable.
- Good hard worker.
- Good at team work.

Project

4th year final project : Real Time system for Control Of Powered Wheel Chair With Head Movement.

M.Tech Final project:- Plasmonic Enhancement Of Efficiency Of Photovoltaic Solar Cells.

Personal Profile

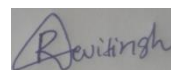
Name: Devisingh
Father’s Name: Budhyanayak
Date Of Birth: 01-Jul-1987
Sex: Male
Marital Status: Married
Nationality: Indian
Languages known: English ,Telugu, Hindi

Declaration:

I hereby declare that all the above-furnished information is correct to the best of my knowledge and belief.

Place: Hyderabad,

Date:



(DEVISINGH)