JNTUH UNIVERSITY

Jawaharlal Nehru Technological University, the First Techno-logical University of India, was established on 2nd October 1972 in Andhra Pradesh with head quarters located in Hyderabad. The University is one of the premier Universities in India, accredited by NAAC with 'A' Grade. After successful and proven levels of appreciated existence and stature spanning over 36 years, JNTU has been divided into four different Universities by Govt. of Andhra Pradesh, through Act No.30, Dt. 24th September, 2008.
JNTU Hyderabad is one among the four Universities. Its Constituent college, "JNTUH College of Engineering, Hyderabad" is regarded as a pioneer in Technical Education and is a flagship College of the University. Other constituent colleges of JNTUH are located at Jagityal, Sultanpur, Manthani and other academic units at Hyderabad campus.

JNTUH College of Engineering

The College was established as Nagarjuna Sagar Engineering College in 1965 by the Government of Telangana. When the college was under the administrative control of the Department of Technical Education, it was affiliated to Osmania University, Hyderabad. With the formation of Jawaharlal Nehru Technological University on 2nd October 1972, it became a constituent college of the University and was later renamed as JNTU College of Engineering, Hyderabad. From its inception in 1965 to 1984, the College was located at Masab Tank Campus. In 1984, the College was shifted to its permanent location at Kukatpally, a 100 acres site, about 20 km from the heart of the City, on Bombay National Highway (NH-9).

Directorate of University Industry Interaction Centre (D-UIIC)

JNTU Hyderabad has been a pioneer in promoting industry-academia interaction and the scope of the activities has been steadily growing. In this endeavour, JNTUH has established a Directorate of University Industry Interaction Centre (UIIC) in the year, 2009.

Industry interactions relating to Engineering and Technology, Basic and Applied Sciences, Pharmacy and Management come under the umbrella of University Industry Interaction Centre. The main focus of UIIC is to bridge the gap between Industry requirements and Academic delivery. The UIIC carries forward the interaction of University with the industrial bodies of Public, Private and Government sector organizations.

About CoreEL Technologies

CoreEL Technologies is a technology company with businesses spread across design services & product development, distribution and training. Head Quartered in Bangalore, India, CoreEL is a leading provider of VLSI & Embedded System design services and Intellectual Property. Since its inception in 1999, CoreEL Technologies a privately held corporation has always strived to deliver quality solutions & support in all the business areas that it serves.

Our Services offerings include Distribution of Silicon solutions, EDA tools, COTS products, Engineering Services (Turn Key Systems Design, Turn Key FPGA Design and High Speed PCB Design), Education and Manufacturing. These services are offered to our broad customer base comprising Defense and Aerospace, Telecommunication and Networking, Homeland Security, Broadcast Video and Education segments.

Pre Requisites:

- Knowledge on Digital IC Design
- Ability to understand Verilog HDL
- Ability Understand C/C++ Language
- Basic Knowledge over FPGAs

Who should attend?

- Practicing Engineers / Faculty

Agenda:

Day 1:

Introduction on VLSI Design & Latest Advancements

- Xilinx FPGA's Architecture Overview (Artix to ZYNQ Ultra Scale Plus :: 45nm to 16nm ICs)
- **Lab : Xilinx Vivado Design Flow (Understanding all features)**
  - Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado design suite. Generate the bit-stream and verify in hardware.
- IP Integrator
- **Lab : Create an Application and Implementing a Hardware Debugging and VIO using the IP Core**
  - Writing the Verilog code for own application
  - Utilizing IP catalog and Creating our Own Application, implementing the same on Hardware
  - Utilizing More I/Os in FPGA (Up-to 256x256)
- **Lab : Application on OLED Display**
  - Writing Verilog/VHDL Code to Display Text/Image on OLED
  - Using 128/32 bit OLED, display the text

Day 2:

- **Lab : Audio DMA Interfacing application** o Using Audio ports in Zed-board o Recording Voice and playing back
- Introduction to Embedded System Design using Zynq
- **Lab : Simple Hardware Design**
  - Create a Vivado project and use IP Integrator to develop a basic embedded system for a target board.
- Zynq Architecture
- Extending the Embedded System into Programmable Logic
- **Lab : Adding Peripherals in Programmable Logic**

- Extend the hardware system by adding AXI peripherals from the IP catalog.
- Writing Application and Debugging using Xilinx SDK

Day 3:

- **Lab : Application using PMODs**
  - Creating Block design Using IP Integrator
  - Adding PMOD WIFI to Block design
  - Running Application on SDK and Controlling Zed-board with Mobile Phone.
- **Lab : Partial Reconfiguration Flow**
  - Use Vivado with Partial Reconfiguration (PR) capability enabled to synthesize HDL models and implement the design.
  - Creating Multiple Bit Files
  - Loading Boot File in SDCard and Programming ZYNQ SOC with SD Card
- **Lab : Demo on Xilinx System Generator Design Flow**
  - Block Design using Simulink and Xilinx Block Sets
  - Creating Hardware Co-simulation
  - Verifying on Zed-board
- **Lab : Demo on Software Defined Radio**
  - Connecting FMC Card to Zed-board
  - Booting Linux OS From Zed-board and Verifying Applications

Key Learning Outcomes:

- Understand the FPGA's and System on Chip
- Current Trends in SOCs
- Practical Knowledge over ZYNQ SOC
- Ability to do Research/Academic Projects on FPGA/SOC
- How to run Partial Reconfiguration
- How to Use Peripherals on ZYNQ SOC and its Applications
- How to integrate MATLAB & Xilinx Tools
- Hands-on Practice over Industry Xilinx Vivado IDE Tools

Chairman:
Dr. E. Sai Baba Reddy, Principal, JNTUH CEH

Co-Chairman:
Dr.Ch.Venkata Ramana Reddy, Director,UIIC, JNTUH

Registration Fee: **There is no Registration Fee**

Registration link:

https://forms.gle/uNTzYrHZB3UJssTn6

Limited seats: Registration is on first come first serve basis. Selected participants will be informed by mail by **11th October, 2019.**

Last date for registration: 10th October, 2019.

Travel/Accommodation

Participants are required to make their own arrangements for travel, local conveyance and accommodation.

Address for Correspondence

Dr. M. Madhavi Latha
Professor
Department of ECE, JNTUH CEH
Cell: 9848506611, Email: mlmakkena@yahoo.com

Venue: Computer Lab, UIIC, JNTUH
Time: 10:00 AM to 5:00 PM

Registration form: Down Load from **jntuh.ac.in**, **jntuhceh.ac.in** websites.

Resource Persons

Mr Suneel Kumar
Associate Manager-Sales Email:
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Mr Nagendra Bandi
Application Engineer
Email: nagendra.b@coreel.com

A 3-Day Faculty Development Program/Short Term Course on

"Designing with ZYNQ SOC and It's Applications"

16-18 October, 2019
(Under TEQIP-III, JNTUH CEH)

In collaboration with
UIIC, JNTUH
and

CoreEL Technologies
Enabling Excellence

Hyderabad

Coordinator
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