JNTUH COLLEGE OF ENGINEERING, HYDERABAD
(AUTONOMOUS)
EXAMINATION BRANCH
NOTIFICATION

Candidates appearing for **M.S in VLSI & Embedded Systems Design (JNTUH & SEERAKADEMI) I & II Semester Supplementary Examinations** commencing from **APRIL, 2015** are informed that the Applications will be received as per time schedule given below:

Last date without late fee	:	20/03/2015
Last date with late fee of Rs.100/-	:	27/03/2015
Last date with late fee of Rs.1000/-	:	02/04/2015
Last date with late fee of Rs.2000/-	:	04/04/2015

(**Theory Exams Commencing on 06-04-2015**)

EXAMINATION FEE:

(a) For Whole Examination: Rs.765/ -

(b) For Supplementary Examination:

i)	Each Theory OR Practical subject	:	Rs. 200/-
ii)	For Memorandum of Marks	:	Rs.10/-
iii)	Cost of Application Form	:	Rs.5/-
iv)	More than Three Subjects (Theory & Practicals)	:	Rs. 765/-

Applications can be obtained from the Examination Branch of the College, from 07/03/2015. The application form along with Bank challan should be submitted in the Examination Branch of the college ON OR BEFORE THE LAST DATES as stated above.

Sd/-

Date:07-03-2015 PRINCIPAL

NOTE:

1. All the students are informed to attach the (Xerox copies) of **CONCERNED SEMESTER MARKS MEMO OF** and College Identity card along with Examination Application Form
2. Copy to the Head of the Department.