JNTUH COLLEGE OF ENGINEERING, HYDERABAD

(AUTONOMOUS)

M.S in VLSI & Embedded Systems Design
(JNTUH & SEERAKADEMI)
II Semester Supplementary Examinations, APRIL, 2015
EXAMINATION TIME – TABLE

Exam Time: 10.00 AM to 1.00 PM

Date	**16/04/2015**
Name of the Subjects	**Analog & Mixed Signal IC Desing**

Sd/-

DATE: 04-04-2015 **PRINCIPAL**